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Sub-nanosecond delay CMOS Active Gate Driver for Closed-Loop d*v*/d*t* Control of GaN Transistors

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***Abstract*— This paper presents an AGD (active gate driver) implemented with a low voltage CMOS technology to control the d*v*/d*t* sequence of low voltage (100V) and high voltage (650V) GaN power transistors. Such an AGD can control and reduce the d*v*/d*t* of fast switching GaN devices with a reduced impact on switching losses. In the case of both low voltage and high voltage GaN fast switching transistors, such an AGD must have a total response time lower than 1ns. Therefore, introducing a feedback loop to control the d*v*/d*t* requires a specific design with a very high bandwidth (550MHz). Moreover, probing the v_{DS} voltage and its derivative is quite challenging, as the voltage level is higher than the low voltage gate driver supply. The purpose of this work is to optimize a low voltage CMOS AGD with fully integrated functions, and implement such a solution in GaN-based power converters.**

Keywords—Active gate driver, GaN, switching analysis, dv/dt, EMI, power electronics, ASIC for power ic.

I. INTRODUCTION

Different solutions have been previously demonstrated to control separately the d*v*/d*t* and d*i*/d*t* sequences with silicon, SiC and GaN FETs in the view of improving the loss versus EMI tradeoff. Different strategies to improve this tradeoff are: a variable impedance output stage, an open-loop control with previously programmed, an adjusted impedance sequence [1-5] or a closed-loop control to reduce the gate current during the d*v*/d*t* sequence [6,7]. The open-loop solutions rely on pre-optimization and fine tuning of the variable impedance switching sequence, which can be sensitive to parameter dispersion [1-5]. Closed-loop controls are either based on discrete components [6,7] or integrated solutions [3]. The discrete solutions typically have a large response time, above few nanoseconds or tens of nanoseconds. Our approach consists to get a full CMOS integration for all the required functions. The size of the high voltage capacitor required to sense the dv_{DS}/d*t* has been reduced to a few pico-Farads, which can be integrated on-chip in our work. This method can be used both for turn-on and turn-off transients. However, the first developments concern only the active control of the turn-on transient. The turn-off sequence is typically controlled by the output load current in the case of high switching speed (low switching losses), and the Zero Voltage Switching (ZVS) condition is more critical than the turn-off switching speed, in the case of synchronous buck converter [8]. However, it should be mentioned that the proposed active gate driver can be easily modified to actively control the turn-off of a fast switching GaN transistors using the exact same principle as the one detailed hereafter.

II. PRINCIPLE OF THE ACTIVE GATE DRIVER

Fig. 1 shows the transistor level schematics of the proposed CMOS AGD. Additionally, to the required output buffer (M5-M6), a high voltage sense capacitor C_S and a two stage current mirror M1-M2 and M3-M4 are integrated. During the d*v*/d*t* sequence, the d*v*/d*t* sense current i_{Cs} is amplified and participates to reduce the gate current i_g during the Miller plateau (Fig. 2). Consequently, the d*v*/d*t* is reduced, while keeping a fast d*i*/d*t* sequence unchanged. The trade-off between d*v*/d*t* and the turn-on energy loss E_{ON} is then optimized, comparatively to a change of the gate resistor R_G, as already demonstrated [6,7].

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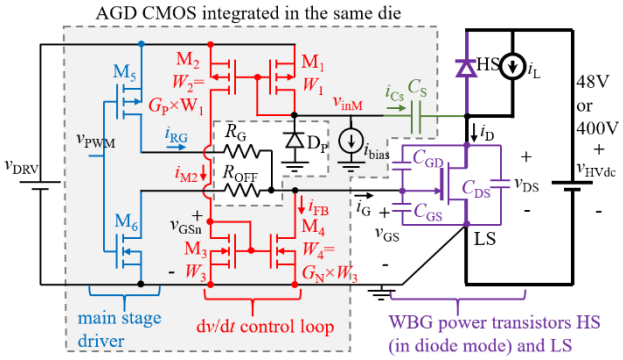


Fig. 1. CMOS AGD topology in a transistor level schematic.

As presented earlier, the transistors M1-M6 are 5V transistors which are particularly suited to drive efficiently EPC GaN transistors, and can also drive GaN systems transistors, albeit with non-optimal driving voltages. The transistors M5 and M6 are designed with a +/-3A source/sink current rating, with integrated pre-amplification and short-circuit protection. D_P is a protection diode to prevent the current mirror input voltage v_{inM} from achieving values outside the safe operating region of the transistor M1. i_{bias} is a current source improving the response time of the feedback loop, which will be further discussed in section IV.

Fig. 2 shows the qualitative current and voltage waveforms during a turn-on of the GaN power device. This time interval can be divided into the di/dt (between t_1 and t_2) and the dv/dt (between t_2 and t_3) sequences. The time duration t_D-t_2 is the feedback loop delay, further analyzed in section IV.

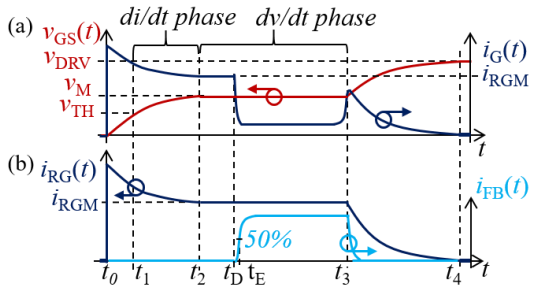


Fig. 2. Qualitative waveforms for gate voltage and currents with the AGD during turn-on (closed-loop). (a) Current and voltage at the power gate and (b) currents being supplied and sinked simultaneously by the AGD.

The main idea of this method is to emulate a virtual capacitor added between the gate and drain nodes of the power device only during the dv/dt phase. The value of such an equivalent capacitor can be controlled by the gain G of the feedback loop (gain of the cascaded current mirrors M1-M2 and M3-M4). One should note that this gain G results from the first stage PMOS transistors and the second stage NMOS transistors $G = G_P \times G_N$. The emulated capacitance effect occurs when a feedback current i_{FB} is sinking from the gate of the power device during the dv/dt phase. This feedback current is generated by the current mirror gain G and the C_S sense capacitor value. This added emulated capacitance equal to GC_S can be easily computed using a simplified model for the power transistor where the dv/dt of the power device is expressed by (1):

$$\frac{dv_{DS}}{dt} = -\frac{v_{DRV}-v_M}{R_G C_{GD}} + \frac{i_{FB}}{C_{GD}} = -\frac{v_{DRV}-v_M}{R_G(C_{GD}+GC_S)} \qquad (1)$$

where v_{DRV} is the power supply voltage of the driver and v_M is the Miller plateau voltage, shown in Fig. 2.

This principle has been previously and successfully applied to the control of Silicon IGBT [6] and high voltage GaN FET [7] for which the turn-on time is significantly high. However, this closed-loop approach is particularly difficult to achieve when GaN

FET are switching within a few nanoseconds. This work aims to demonstrate experimentally the feasibility and the limitations of such an AGD with both low voltage and high voltage GaN FETS, thanks to a full CMOS integration.

TABLE I. COMPARISON OF PERFORMANCE FOR THE SAME METHOD OF DV/DT CLOSED-LOOP CONTROL

	Published by [6]	***Published by [7]***	***This work***
Reduction in | dV/dt |	1.8 to 0.5V/ns	27 to 8V/ns	45 to 6.6V/ns
v_{HVdc}	600V	300V	400V and 48V
v_{DS} fall time during turn-on	333ns	11ns	20ns and 4ns
Embedded in an ASIC	No	No	Yes

III. IMPLEMENTATION

A. CMOS AGD

Fig. 3 shows a microscope photograph of the fabricated AGD in AMS 180nm CMOS technology. This first prototype has been designed as a test chip with several current mirror designs and embedded high voltage capacitors. Even though quite simple, the design of the current mirrors is subject to important compromises such as the feedback loop gain splitting between the C_S value, the first and second current mirror stage gain values, the large maximum output current in M4, the dynamic bias current i_{bias} and the M2-M3 biasing during the active driving. Key constraints are current consumptions, total silicon area (embedded capacitor + current mirrors) and bandwidth. These design considerations will be illustrated in section IV. After a quick characterization in probe station [9], the AGDs are packaged in QFN24 6mm×6mm. The packaged AGDs are then implemented to drive commercially available low voltage and high voltage GaN FETs.

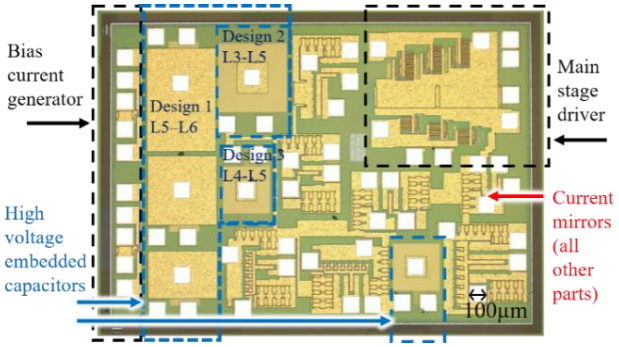


Fig. 3. Optical microscope photograph of the CMOS AGD test chip built in 0.18µm technology.

B. Implementation in 48V and 400V DC bus voltages

Two different boards have been developed to demonstrate the active control of GaN transistors in 48V and 400V applications. In both experiments, only the low side (LS) GaN transistor is driven by our CMOS AGD, while the high side (HS) GaN transistor has its gate and source shorted. The 4-layer PCB (48V) and 6-layer PCB (400V) have been designed to minimize the gate and power loops, hence only voltage probes are used. In this first implementation, an external C_S ceramic capacitor is used, 2pF/250V for 48V (J0603D2R0BXPAJ) and 1pF/500V for 400V (MC0805N1R0C501CT).

Fig. 4 (a) shows the system implementation in a 48V-36A power commutation cell with EPC2001 eGaN™FET. Fig. 4 (b) shows a similar implementation in a 400V-30A application, with GaN systems e-mode GS66508T transistors. Additional components are limited to decoupling capacitors, protection and configuration buffers and gate resistors.

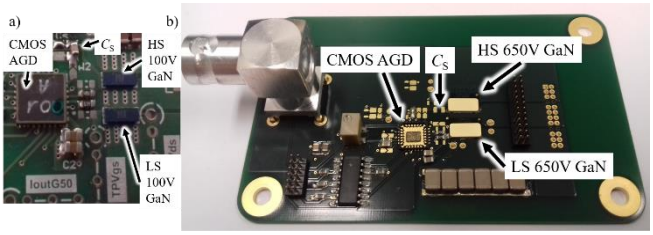


Fig. 4. AGD in a half bridge configuration for test in double pulse for (a) 4-layer board with 48V DC bus voltage with 100V GaN EPC 2001C device. (b) 6-layer board with 400V DC bus voltage with 650V GaN systems GS66508T devices.

C. Experimental Results

In the case of 48V bus voltage, the d*v*/d*t* is attenuated from 15V/ns to 6.3V/ns with the CMOS AGD (Fig. 5). Simulation results shows the switching losses are increased from 1.93µJ to 2.34µJ during turn-on. Cadence™ simulation results fitting experimental data shows the switching losses are reduced by 15.7% comparing to the increase of the gate resistance R_G, while keeping the same attenuation in d*v*/d*t*. For the 400V application, the d*v*/d*t* is attenuated from 45V/ns to 6.6V/ns, (Fig. 6). Both cases use $R_G = 4.4\Omega$. This choice of R_G has been made for the EPC2001C because characterization tests in open-loop with lower values showed no more significant increase in peak d*v*/d*t* with lower R_G values. For 400V tests, the same value is used for comparative purposes.

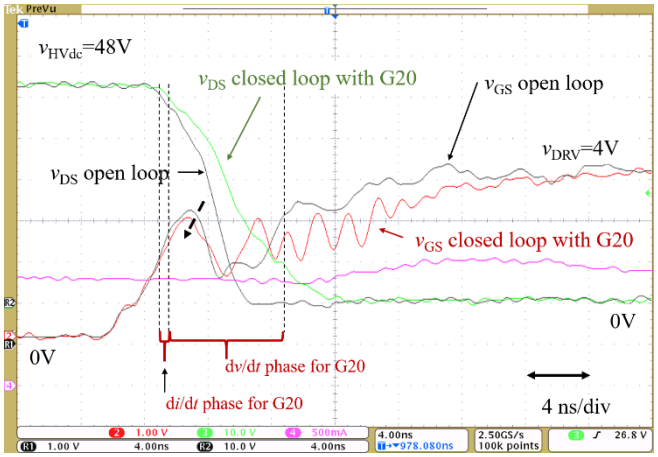


Fig. 5. Experimental results with the CMOS AGD in the 48V DC bus voltage. With the closed-loop, the d*v*/d*t* is attenuated from 15V/ns to 6.3V/ns.

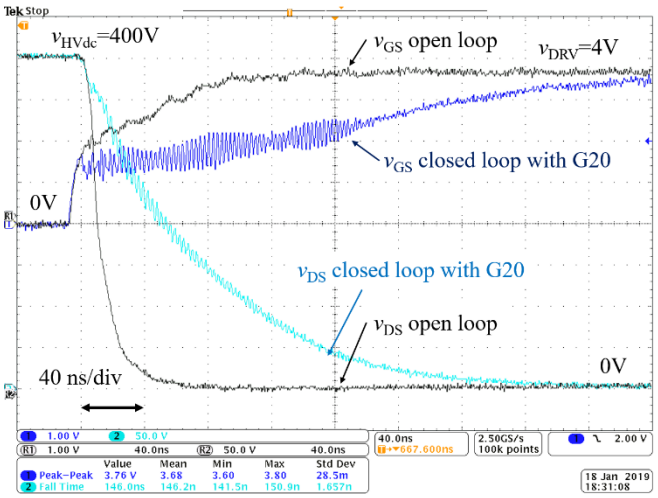


Fig. 6. Experimental results with the CMOS AGD in the 400V DC bus voltage. With the closed-loop, the d*v*/d*t* is attenuated from 45V/ns to 6.6V/ns.

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IV. Response Time of the Feedback Loop

A. *Reducing the delay time by pre-biasing the current mirrors*

One way to reduce the delay of the feedback loop (t_D-t_2) is to pre-bias the current mirrors M1-M2 and M3-M4 by pre-charging their capacitors with a low biasing current i_{bias}. Doing so, the pre-biased transistors, biased in their linear region, are able to provide a very fast response for any external transient. Table I shows the results obtained with Cadence™-Spectre™ transient simulations to determine the value of the delay defined in Fig. 2 for different biasing currents i_{bias}. Different total gain values (5, 10, 20 and 50) for the current mirrors are simulated and implemented within the prototype. One has to note that all transistors M1-M4 are designed differently for each case of total gain G value. If different gain modifies the dv/dt in closed-loop and consequently the input current i_{Cs}, it also implies different parasitic capacitance values which impact the overall response time. In these simulations, for comparison purpose, a constant dv/dt equal to 15V/ns with a sense capacitor of 2pF is considered. The design must be done carefully, splitting the total gain G into two different gain G_P and G_N to minimizing the parasitic capacitors of the transistors, leading to an optimized size reducing the several time constants of the feedback loop.

TABLE II

SIMULATED RESPONSE TIME FOR DIFFERENT

VALUES OF BIASING CURRENT WITH THREE DIFFERENT GAINS

	G10 pre-biased		**G20 pre-biased**		**G50 pre-biased**	
bias *current*	*Time delay*	*50% settling time*	*Time delay*	*50% settling time*	*Time delay*	*50% settling time*
i_{bias}	t_D-t2	t_E- t_D	t_D-t2	t_E- t_D	t_D-t2	t_E- t_D
0	218ps	214ps	244ps	279ps	351ps	503ps
20µA	80ps	256ps	83ps	337ps	102ps	608ps
2mA	27ps	251ps	28ps*	330ps*	31ps	589ps

* shown in Fig. 7

The time intervals t_D–t_2 and t_E–t_D are determined on Fig. 7 showing a simulation of the response time with the current mirror G = 20 pre-biased with a 2mA i_{bias} current. The input current goes from 0 to 26mA that correspond to a dv/dt equal to either 26V/ns with C_S = 1pF or 13V/ns with C_S = 2pF.

After tens of picoseconds the feedback loop provides a current at the output (i_{FB}) and therefore is already acting and affecting the dv/dt.

The delay decreases as the bias current i_{bias} increases. This improvement is at the expense of an additional power consumption. Indeed, using a pre-bias current, extra losses in transistors M1 to M4 are generated, which can reach high levels due to the high value of the gain G_P. It should be noted that, this biasing current can be provided only during the switching. Then, a trade-off between extra losses and bandwidth improvement has to be considered.

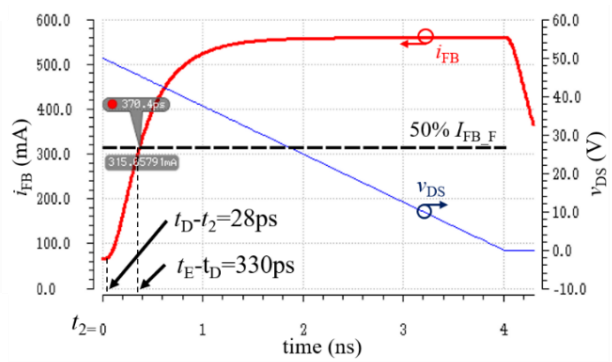


Fig. 7. Simulation of the transient response time with G = 20 (v_{DRV} = 4V, i_{bias} = 2mA, i_{Cs} = 30mA).

B. Bandwidth analysis

If a non-null current i_{bias} is used to pre-bias the two current mirrors, a small signal analysis can be performed to determine the bandwidth of the feedback loop. Fig. 8 shows the equivalent circuit required for the study in the frequency domain. The input signal is the current coming from the capacitor C_S during a turn-on event assuming that a constant dv/dt occurs during the transient. The output of the second stage is connected to the resistance R_G and the gate of the power device behaving like a voltage-dependent capacitor C_{ISS} during the Miller's plateau. Small signal models of transistors M1 to M4 are used in Fig. 8:

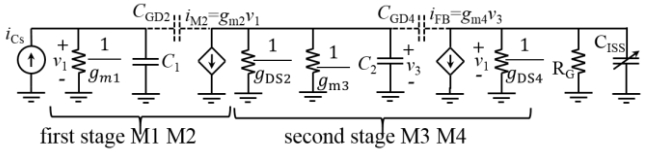


Fig. 8. Small signal analysis of the AGD current mirrors during dv/dt phase.

The current gain transfer function is expressed by (2).

$$\frac{I_{FB}(s)}{I_{Cs}(s)} = G_P G_N \frac{1-\frac{C_{GD2}s}{g_{m2}}}{1+\tau_{21}s} \cdot \frac{1-\frac{C_{GD4}s}{g_{m2}}}{1+\tau_{43}s} \quad (2)$$

where G_P and G_N are respectively the gains of the current mirrors M1-M2 and M3-M4, g_{mi} and g_{DSi} respectively the transconductances and the drain-to-source admittances of transistors M1 to M4, τ_{21} and τ_{43} the time constants of both current mirrors.

The mirror time constants are calculated with the following expressions:

$$\tau_{21} = \frac{C_1}{g_{m1}};\ \tau_{43} = \frac{C_2}{g_{DS2}+g_{m3}} \quad (3)$$

with

$$\begin{cases} C_1 = C_{DP} + C_{DS1} + C_{GS1} + C_{GS2} + C_{GD2}\left(1 + \frac{g_{m2}}{g_{DS2}+g_{m3}}\right) \\ C_2 = C_{DS2} + C_{DS3} + C_{GS3} + C_{GS4} + C_{GD4}\left(1 + \frac{g_{m4}}{g_{DS4}+\frac{1}{R_G}}\right) \end{cases} \quad (4)$$

where C_{DP} is the capacitive contribution of the reverse biased protection diode D_P.

A Cadence™ AC simulation (Fig. 9) demonstrates a bandwidth close to 550MHz (-3dB gain) for the two-step current mirror with a current gain G = 20 and considering an input current made of a biasing current i_{bias} = 2mA increased by a 12mA current generated by a constant dv/dt equal to 6v/ns in a sensing capacitor C_S = 2pF.

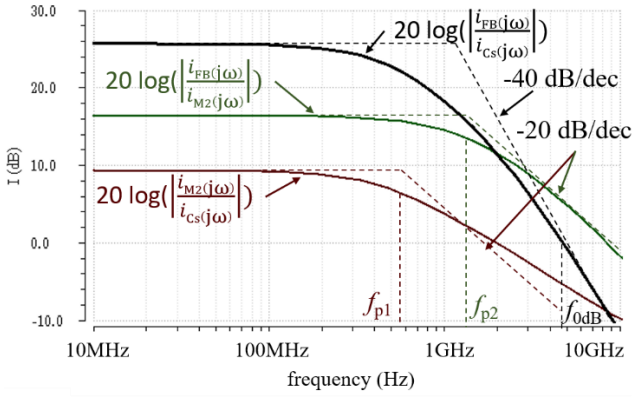


Fig. 9. Cadence™ simulation of the two-step current mirror transfer function (i_{bias} = 2mA, dv/dt = 6V/ns, G = 20, CMOS 0.18µm technology).

With this large bandwidth, the step response of the cascaded mirrors provides a settle time equal to $(t_E\text{-}t_D)_{50\%}$ = 220ps that is close to the result provide on table II.

V. Embedded Capacitor for dv/dt Sensing

In order to propose a fully integrated solution, high voltage pF range C_S capacitors are integrated on chip. The different designs involve different metal and oxide layers offered by the CMOS technology. The design compromises are the capacitor density, the breakdown voltage and the common mode parasitic capacitor. The breakdown voltages of three different designs are measured between 500V and 3.5kV (Fig. 10). The measurements have been done in a probe station under vacuum. For low voltage applications (48V), 5.5pF are measured with a surface of 0.13mm² and a destructive breakdown at 450V. For medium voltage applications (400V), 1.3pF to 2.9pF are measured for a surface of 0.19mm² to 0.35mm² respectively. The destructive breakdown for those capacitors occurs at 3.5kV. These measurements confirm the viability of a full CMOS integration of our solution.

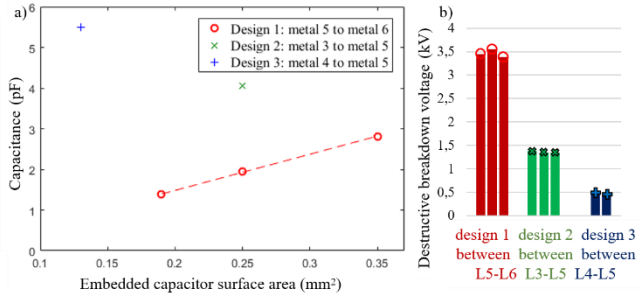


Fig. 10. High voltage embedded capacitor integration measurements for the proposed method (a) capacitance (b) breakdown voltage (L3 to L6 are the metal layer of the technology).

VI. Conclusion

A solution to reduce the dv/dt value while saving switching loss is presented and fully integrated in CMOS technology. 15.7% E_{ON} switching energy is saved compared to a simple reduction in dv/dt by changing the gate resistance. A high bandwidth is demonstrated both theoretically and experimentally for the feedback loop, showing sub-nanosecond delays. The experimental characterizations show the effectiveness of the active dv/dt control of fast switching GaN power transistors both for 48V and 400V applications. The key benefits of our technique are: a fully CMOS integrated solution, a reduced overcurrent during turn-on, an improved EMI vs switching-loss tradeoff, simple and fast analog circuits to implement a closed-loop technique and the possibility to integrate pF range high voltage capacitor used as a dv/dt sensor. Next steps will be the integration of continuously variable feedback gains and further optimization both in design and topology.

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