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Scalable compact modeling of trap generation near the EB spacer oxide interface in SiGe HBTs

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Abstract

This paper presents a physics-based scalable formulation for interface trap generation in the vicinity of the emitter-base spacer oxide interface in advanced SiGe HBTs. Aging tests were performed for various emitter dimensions to investigate the scalability of the dynamics of hot-carrier degradation. An improved formulation of the bond dissociation rate is also proposed incorporating a scaling rule depending on the avalanche current density. The hydrogen diffusion through the EB spacer has been modeled using an RC ladder network and has been scaled according to the hydrogen diffusion volume. Its accuracy has been validated over a wide range of aging tests and various geometry features.

Keywords: SiGe HBTs, reliability, compact model, hot-carrier degradation, hydrogen diffusion

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1. Introduction

Due to the drastic miniaturization of electronic devices [1], electrical performances of advanced SiGe heterojunction bipolar transistors (HBTs) are constrained in terms of safe-operating-area (SOA). Over the last decades, the collector-emitter breakdown voltage (BV_{CEO}) has decreased significantly to meet the demand of continuously increasing cut-off frequencies, thus limiting the available output power. Therefore, modern circuits are being forced to operate at higher voltages where hot-carrier degradation (HCD) mechanism is predominant. This degradation mechanism is now well known in SiGe HBTs where the hot-carriers created by impact ionization can reach the emitter-base (EB) spacer oxide interface, leading to the dissociation of the passivated Si-H bonds [2, 3, 4, 5]. The main electrical issue induced by HCD is the increase of the base current at low and moderate injection levels which thereby causes a large decrease of the current gain β as well as a degradation of the low-frequency noise [2].

Since HCD is a consequence of the impact ionization mechanism [6], the resulting avalanche current has to be accurately predicted at low and high current densities. A formulation for the avalanche multiplication factor has recently been proposed in [7] for extending the validation range of the avalanche multiplication factor up to high current densities. Thus, the extraction flow of the aging compact model parameters must start with an accurate extraction of the associated new avalanche parameters.

As pointed out in [8], some of the degradation attributes, such as the saturation value of the aging-induced shift in the base current or the degradation dynamics, are SiGe HBT architecture-dependent. Indeed, as demonstrated for the universality of HCD in MOSFET architectures [9], the degradation magnitude for SiGe HBTs will widely depend on the emitter dimensions [10], the Si/SiO₂ interface quality as well as the spacer morphology. Through a first set of results, [11] demonstrates that the trap generation along the interface is quite uniform, meaning that the entire interface-spacer surface suffers from the bond dissociation. Thus, the dimensions of this surface plays an important role in the evolution of degradation.

The preceeding version of the aging compact model proposed in [8] (HiCuM AL V2.0) has demonstrated good accuracy compared to the measurements under both static and dynamic stress conditions. Since a circuit is often designed using different device geometries, a scaled formulation for HCD appears to be the next step necessary toward circuit reliability simulation. A scalable aging model has already been proposed in [10]

which is based on a different physical background, the lucky electron model.

In continuation of our previous approach, the current paper introduces an extension of the previous aging compact model (HiCuM AL V2.0) presented in [8] incorporating the new scaling rules developed in accordance with the emitter dimensions and the EB spacer morphology (HiCuM AL V3.0). The rest of this paper is organized as follows; Section II focuses on the physical origin of hot-carrier degradation studied through electrical measurements and TCAD based simulations; Section III demonstrates the scalability of the degradation mechanism using various emitter dimensions; Section IV describes the scalable compact model formulation and the hydrogen diffusion mechanism; Section V presents an extraction procedure for the aging model parameters; Section VI validates the simulation results for a wide range of aging tests and devices under test (DUTs).

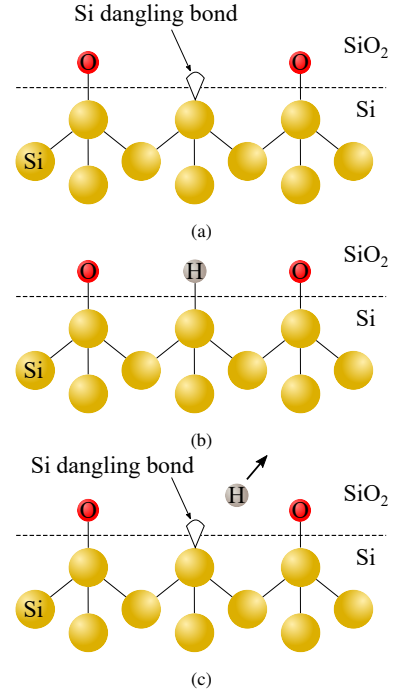


Figure 1: (a) Si dangling bond creation at the Si/SiO₂ interface, (b) Incorporation of hydrogen atoms for passivation of dangling bonds and (c) Interface trap creation and hydrogen diffusion due to hot-carrier mechanism

2. Physical origin of hot-carrier degradation

2.1. Description

The structural disorders at the Si/SiO₂ interface lead to the creation of silicon dangling bonds as illustrated

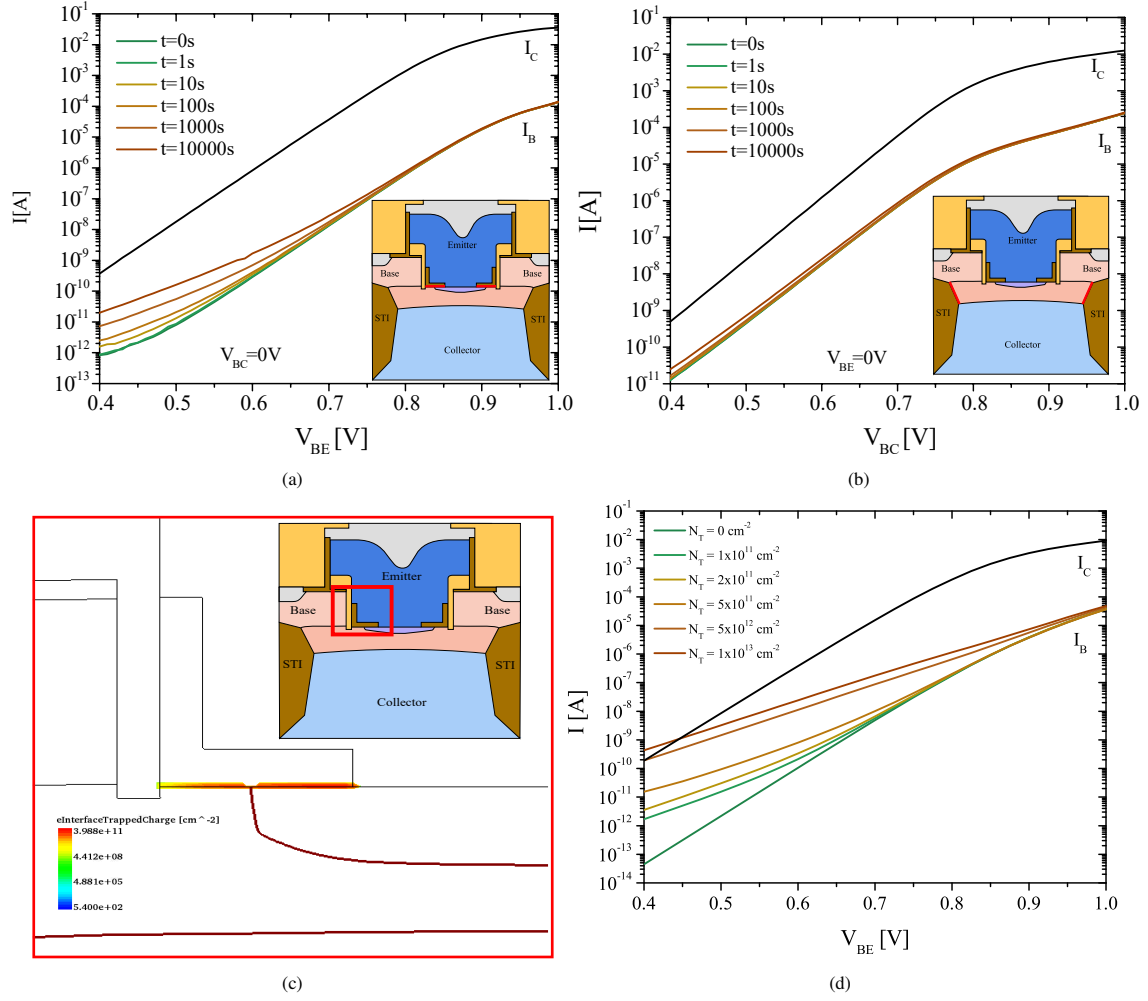


Figure 2: (a) Forward and (b) Reverse Gummel plots for a stress condition of $V_{CB} = 2V$ and $J_E = 0.46 \text{ mA}/\mu\text{m}^2$ at different stress times, (c) TCAD structure from the inset [12] showing the addition of traps at the EB spacer interface and (d) corresponding TCAD electrical simulations results for various trap densities

in figure 1a. In order to reduce carrier-trapping in this particular region, these dangling bonds are passivated by integrating hydrogen atoms [13], as illustrated in figure 1b. However, due to low binding energy of Si-H bonds (2.3eV compared to 3.1eV for Si-O₂ bonds [14]), hot-carriers can gain sufficient energy to break these passivated bonds. The remaining Si dangling bonds can thus act as interface traps while the hydrogen released from these bonds diffuse away from the interface, as shown in figure 1c. In SiGe HBTs, these trap states can be located at the EB spacer or at the Shallow-Trench-Isolation (STI) oxide interface which produces an excess non-ideal base current through the Shockley-Read-Hall (SRH) recombination [13].

2.2. Traps location

Since two regions can possibly be impacted by HCD, a dedicated set of measurements must be set up to discriminate the traps created at the EB spacer from the ones created at the STI. Thus, mixed-mode aging tests have been performed on a 55nm BiCMOS technology with several in-between measurements of forward (see figure 2a) and reverse (see figure 2b) Gummel plots.

In figure 2a, a large increase of the base current is observed that implies the creation of traps near the BE junction. On the contrary, the weak increase of the base current in figure 2b indicates that the trap creation close to the BC junction is less significant. Therefore, the region that principally contributes to the increase of the base current is the EB spacer oxide interface.

Complimentarily, TCAD simulations [4] were performed on a simulated structure featuring this technology where various trap densities N_T were introduced at the EB spacer interface, as shown in figure 2c. As observed from the forward Gummel TCAD simulations in figure 2d, introducing traps in the EB spacer region leads to an increase of the base current at low V_{BE} (while the collector current remains unchanged) which is consistent with the aging test results.

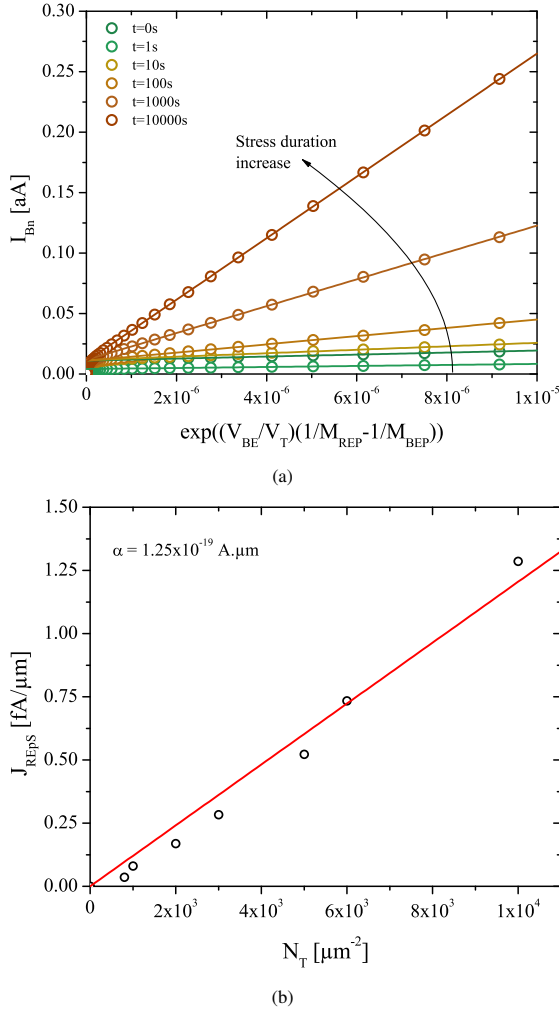


Figure 3: (a) Normalized base current at emitter periphery, I_{Bn} , extracted from measurements for a stress condition of $V_{CB}=2V$ and $J_E=0.46mA/\mu m^2$ at different stress times and (b) J_{REpS} evolution extracted from TCAD simulations allowing the extraction of the proportionality coefficient α

2.3. Compact model analysis

From the point of view of compact models such as HICUM [15], the creation of traps at the Si/SiO₂ interface can be attributed to the modification of a specific

base current parameter, the peripheral B-E recombination saturation current. Since only the region around the emitter periphery is impacted by HCD, the effect of degradation in the internal base-emitter current parameters can be neglected. Thus, the base current under forward operation conditions outside the avalanche regime can be expressed by equation (1) [15].

$$I_B = I_{BEPs} e^{\left(\frac{V_{BE}}{M_{BEP} V_T} - 1\right)} + I_{REpS} e^{\left(\frac{V_{BE}}{M_{REP} V_T} - 1\right)} \quad (1)$$

where I_{BEPs} is the peripheral B-E saturation current, M_{BEP} is the peripheral B-E current ideality factor, I_{REpS} is the peripheral B-E recombination saturation current and M_{REP} is the peripheral B-E recombination current ideality factor.

A normalized expression of the base current, I_{Bn} , is obtained using equation (2). From the measurements presented in figure 2a, the I_{Bn} parameter is extracted at different stress duration and is plotted against $e^{\left(\frac{V_{BE}}{V_T} \left(\frac{1}{M_{REP}} - \frac{1}{M_{BEP}}\right)\right)}$ in figure 3a. As observed from this plot, while the point of intersection of the linear regression lines remains the same, the slope increases with stress time. Therefore, the parameter impacted by HCD, following equation (2), is the parameter I_{REpS} [4, 8, 10].

$$I_{Bn} = \frac{I_B}{e^{\left(\frac{V_{BE}}{M_{BEP} V_T} - 1\right)}} = I_{BEPs} + I_{REpS} e^{\left(\frac{V_{BE}}{V_T} \left(\frac{1}{M_{REP}} - \frac{1}{M_{BEP}}\right)\right)} \quad (2)$$

In addition, we used TCAD simulations together with HICUM simulations to correlate the increase of I_{REpS} with that of the density of traps at the spacer interface for a given geometry. To develop a scalable formulation of the degradation mechanism, the I_{REpS} parameter has been converted to J_{REpS} normalizing by the emitter perimeter P_E . The results are displayed in figure 3b for various trap densities depicting a linear relation between N_T and J_{REpS} which can be expressed by equation (3).

$$J_{REpS}(t) = \alpha N_T(t) \quad (3)$$

where α is the proportionality coefficient extracted from the linear regression of figure 3b. This formulation introduces a geometry dependent expression for I_{REpS} as presented in equation (4).

$$I_{REpS}(t) = \alpha P_E N_T(t) \quad (4)$$

3. Scalability of degradation mechanism

3.1. HBT under test

Figure 4 shows the morphology of the EB spacer for the technology under test. The area of the EB spacer

interface (in red), A_{SPACER} , depends on the effective emitter length, L_E , the effective emitter width, W_E , and the EB spacer width, d_{SP} .

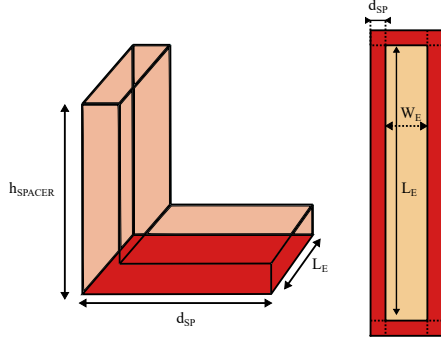


Figure 4: Side and top view of the emitter-base spacer of 55nm technology

W_E [μm]	L_E [μm]	A_{SPACER} [μm^2]
0.09	4.8	0.39
0.09	8.8	0.79
0.09	17.8	1.60

Table 1: Geometry features of devices under test

The interface area, A_{SPACER} , expressed in equation (5), largely depends on the emitter perimeter P_E which is consistent with the degradation region identified in the previous section. The dimensions of the DUTs are presented in table 1 summarizing the corresponding geometry features.

$$A_{SPACER} = 2d_{SP}(L_E + W_E + 2d_{SP}) \simeq P_E d_{SP} \quad (5)$$

3.2. Stress conditions

In order to verify the scalability of the hot-carrier mechanism, each device has been biased under the same stress conditions, e.g. a constant base-collector voltage V_{CB} and a constant emitter current density J_E at an ambient temperature of 25°C. The stress conditions for the three DUTs are presented in figure 5a : various V_{CB} s ranging from 1.5V to 2.7V were used to induce the electric field effect on HCD whereas various J_E s ranging from 200 $\mu\text{A}/\mu\text{m}^2$ to 50 $\text{mA}/\mu\text{m}^2$ were applied which thus led to the increase in the device temperature (T_j).

Each stress condition (summarized in table 2) was carefully chosen outside the pinch-in area in order to avoid thermal and electrical instabilities [16]. Devices were submitted to aging tests for 10ks with intermediate Gummel measurements in logarithmic time intervals.

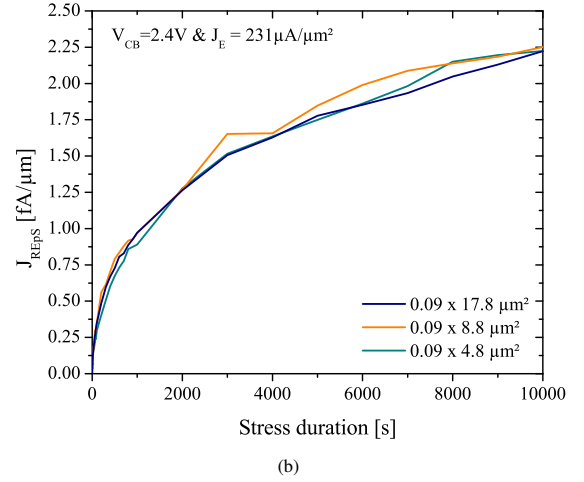
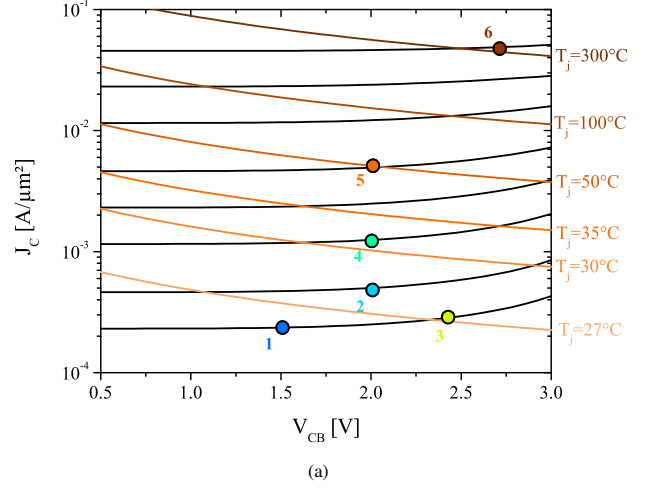


Figure 5: (a) $J_C - V_{CB}$ curves illustrating the stress conditions applied on the three DUTs for $T_{AMB}=25^\circ\text{C}$ and (b) J_{REPS} extraction for a stress condition of $V_{CB}=2.4\text{V}$ and $J_E=231\mu\text{A}/\mu\text{m}^2$

3.3. Measurement results

Alike the results presented in previous studies [8, 17, 18], the I_{REPS} parameter of HICUM compact model has been extracted for each DUTs and each stress conditions (for V_{BE} ranging from 0.5V to 0.7V). The maximum values obtained for this parameter at $t=10\text{ks}$ is equal to 22fA for the smallest and 80fA for the largest geometry, respectively. Thus, the number of created traps is greater for larger devices due to the increase of the A_{SPACER} area.

The J_{REPS} 's (I_{REPS} parameter normalized by P_E) evolution is plotted as a function of the stress time in figure 5b. Interestingly, from this plot, it is noticeable that the values of J_{REPS} are identical for each DUT implying that the degradation mechanism is scalable with the emitter perimeter. Similar results were obtained for the other

Number	V_{CB} [V]	J_E [mA/ μm^2]	T_j [°C]
1	1.5	0.23	25
2	2	0.46	27
3	2.4	0.23	25
4	2	1.2	31
5	2	4.6	45
6	2.7	47	315

Table 2: Details of the stress conditions depicted in figure 5a

stress conditions.

4. Model formulation

4.1. Reaction-diffusion theory

The bond dissociation rate can be calculated following the reaction-diffusion theory [19] as represented by equation (6).

$$\frac{dN_T}{dt} = K_F(N_F - N_T(t)) - K_R N_T(t) N_H(0, t) \quad (6)$$

where K_F is the trap generation rate, K_R is the trap annihilation rate, $N_T(t)$ is the density of created traps at the interface, N_F is the density of available bonds that can break and $N_H(0, t)$ is the volumetric density of hydrogen remaining at the Si/SiO₂ interface.

Following the proportionality established between N_T and I_{REPS} in section II, the compact model implementation has slightly been modified compared to [8]. In this work, it is the trap density N_T which is dynamically calculated using equation (6) while I_{REPS} parameter is determined using equation (4).

An extraction procedure for K_F , K_R and N_F is required to obtain an accurate model response for a single device, which will be presented in section 5. However, the hydrogen diffusion dynamics must be well formulated before, in order to accurately calculate the number of hydrogen atoms remaining at the Si/SiO₂ interface.

4.2. Diffusion mechanism

As presented in section 2.1, the free hydrogen atoms created due to the hot-carrier mechanism diffuse away from the EB spacer oxide interface and are primarily stored within the spacer oxide. The hydrogen atoms could further diffuse beyond the spacer, through the emitter poly-Si, as illustrated in figure 6a, depending on the diffusion dynamics. This last mechanism is governed by the hydrogen diffusion coefficient D_H (through D_0 and E_a [8]) which is material-dependent as summarized in table 3.

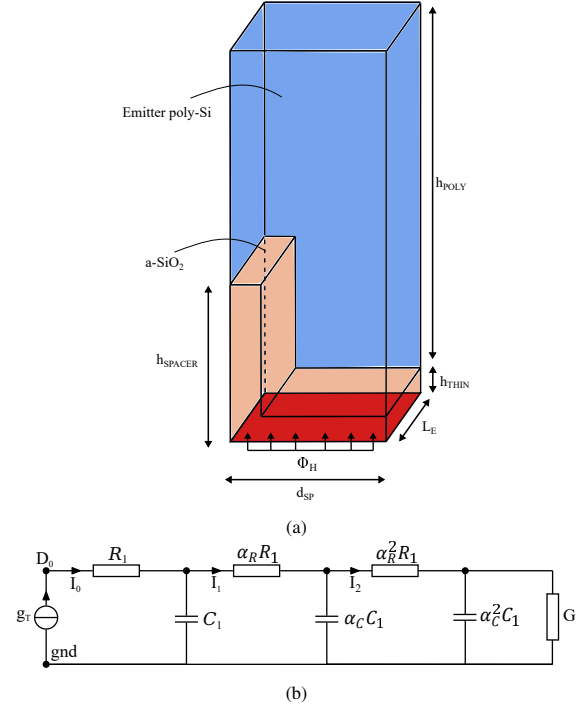


Figure 6: (a) Schematic of the hydrogen diffusion volume taking into account the EB spacer oxide and the emitter poly-Si thickness and (b) RC ladder network for hydrogen diffusion modeling

In this table, three materials are considered : the amorphous SiO₂ (a-SiO₂) located in the EB spacer, the highly-doped (N-type) poly-crystalline Si (poly-Si) in the emitter and the crystalline Si (c-Si) which is the material reference. For each material, the table lists the hydrogen diffusion parameters and the corresponding diffusion length calculated from equation (7) with a diffusion time $t_D = 1$ s and $T=300$ K. Since the hydrogen diffusion coefficient follows an Arrhenius law, the diffusion length for different materials varies at higher temperatures.

$$L_D = \sqrt{4D_H t_D} \quad (7)$$

Type	D_0 [$\mu\text{m}^2/\text{s}$]	E_a [eV]	L_D [μm] (7)
a-SiO ₂ [20]	1×10^4	0.18	6.15
poly-Si [21]	1×10^{-2}	0.35	2.30×10^{-4}
c-Si [22]	1×10^6	0.48	0.185
This work	4.64×10^{-1}	0.48	1.26×10^{-4}

Table 3: State-of-the-art for hydrogen diffusion parameters in various materials and their corresponding diffusion length L_D for $t_D=1$ s and $T=300$ K

From table 3, it is evident that the hydrogen atoms diffuse significantly slower in the poly-Si compared to

the other two materials since its grain boundaries acts as efficient traps [23]. Thus, the hydrogen atoms are drastically accelerated within the thin SiO₂ layer until they reach the thicker poly-Si layer where it would be harder to diffuse further efficiently. Considering the time scale used for measurements, the diffusion inside the spacer is not observable since it only takes a few μ s to cover a few tens of nanometers. As a consequence, the current work focuses on the long-term hydrogen diffusion that takes place inside the poly-Si.

4.3. Diffusion model

Based on Fick's law of diffusion [24], the hydrogen diffusion from the Si/SiO₂ interface beyond the EB spacer oxide can be modeled using a RC ladder network, similar to the approach adopted for thermal analysis [25]. The corresponding equivalent circuit is presented in figure 6b where the diffusion volume is divided into N cells; here we have considered N=3 for the technology under test. A conductance G has been added at the end of the recursive network to model the long-term behavior (e.g. the diffusion of hydrogen beyond the poly-Si). Each resistance and capacitance of the network is calculated using equation (8).

$$\begin{cases} C_n = C_H \frac{\alpha_C^{n-1} - \alpha_C^n}{1 - \alpha_C^n} \\ R_n = R_H \frac{\alpha_R^{n-1} - \alpha_R^n}{1 - \alpha_R^n} \end{cases} \quad (8)$$

where C_H represents the storage capacity of hydrogen atoms in μ m, R_H represents the barrier to normal lattice diffusion [26] in μ m⁻¹.s, α_C and α_R are the recursive factors for the capacitances and the resistances, respectively.

Following the assumptions made in section 4.2, the equivalent diffusion volume V_{DIFF} is only composed of the emitter poly-Si leading to equation (9).

$$V_{DIFF} = h_{POLY} A_{SPACER} \quad (9)$$

Thus, following the definition of C_H parameter, a scalable formulation can be obtained as shown in equation (10), that depends on the diffusion volume of hydrogen (V_{DIFF}) and the interface trap generation surface (A_{SPACER}). Furthermore, the R_H parameter is calculated using the diffusion constant of hydrogen, D_H , in the considered material as also depicted in equation (10).

$$C_H = \frac{V_{DIFF}}{A_{SPACER}}, R_H = \frac{C_H}{D_H} \quad (10)$$

5. Parameter extraction procedure

5.1. Density of Si-H bonds at the interface

The bond dissociation is a first order mechanism represented by the first term of equation (6) in which the values of N_F and K_F have to be evaluated. The first one can be extracted from the maximum value of J_{REPS} obtained for the three devices, since it is directly related to the maximum number of traps that can be created at the interface. As observed from the aging test results the saturation of the degradation characteristics [8] has not been reached after 200ks for the stress condition presented in figure 7a. Therefore, the maximum value of J_{REPS} has been extrapolated to $J_F=6$ fA/ μ m leading to equation (11) from which N_F can be extracted for a given technology.

$$N_F = \frac{J_F}{\alpha} \quad (11)$$

where α is the coefficient extracted in section 2.3.

5.2. Generation rate

The second parameter, K_F , is extracted when no annealing process can yet be observed and when the number of created traps (e.g. N_T) is close to 0. Thus, equation (6) becomes equation (12) where the K_F can be extracted from the slope of dJ_{REPS}/dt with known values of the N_F and α parameters. The aging range of time for the parameter extraction has been limited by defining a maximum deviation of 1% for J_{REPS} compared to its maximum values, J_F .

$$\frac{dJ_{REPS}}{dt} = K_F N_F \alpha \quad (12)$$

An example of the extraction method is shown in figure 7b while the extraction results obtained under five different stress conditions for a device geometry of $0.09 \times 4.8 \mu$ m² is presented in figure 7c. From this figure, an expression of K_F has been formulated as functions of J_{AVL} and V_{CB} . Indeed, in [3, 8, 10], the decline of K_F parameter at large current densities is due to the reduction of J_{AVL} as demonstrated in [7].

For this reason, the expression of K_F has been modified by introducing the J_{AVL} parameter which can be obtained using the new avalanche model [7] as,

$$J_{AVL} = \frac{I_{AVL}}{A_{AVL}} \quad (13)$$

where I_{AVL} is the avalanche current and A_{AVL} is the effective emitter area for the avalanche current [27]. The detailed extraction procedure for the avalanche effect

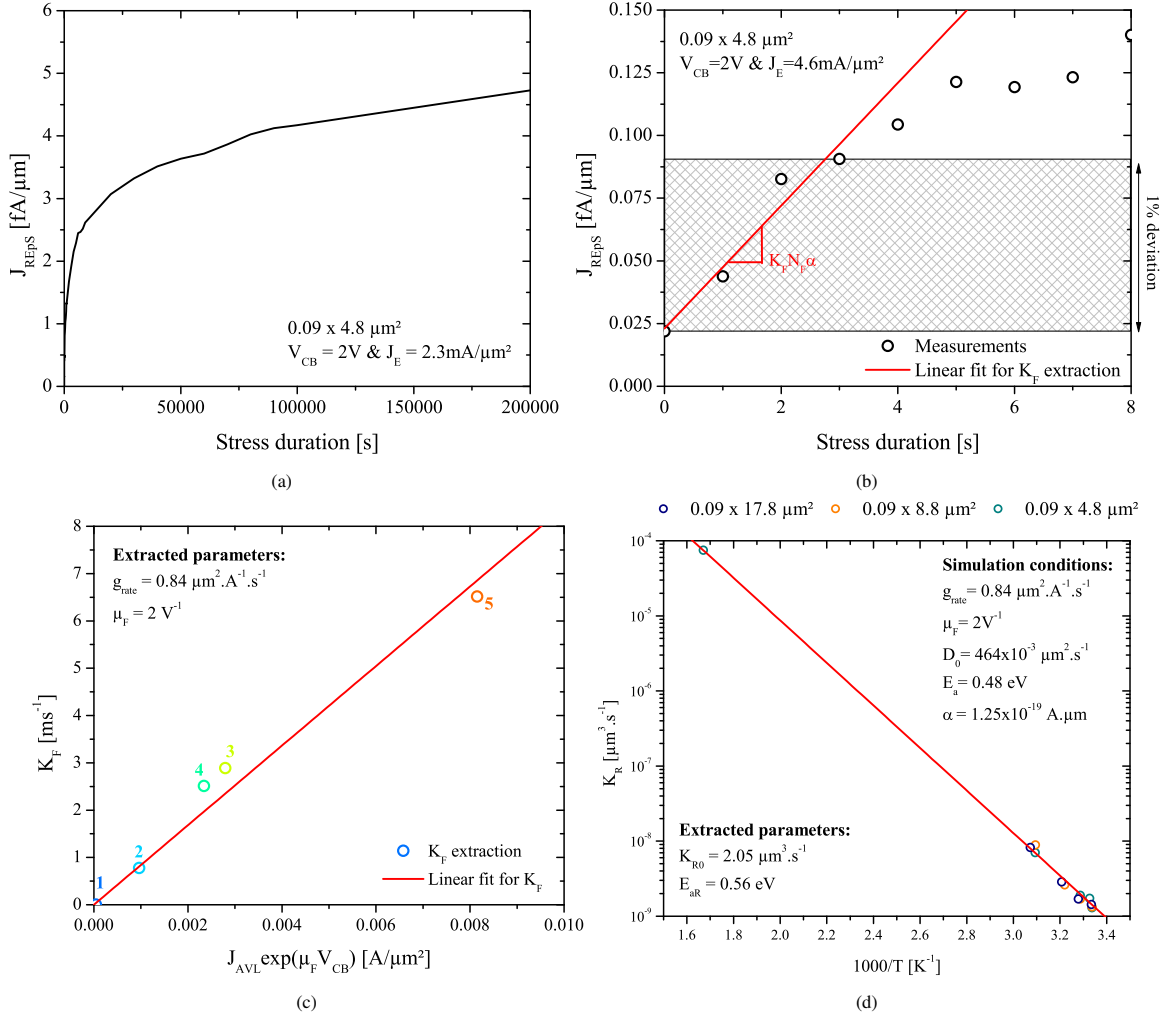


Figure 7: (a) Evolution of J_{REPS} for a long stress duration which allows the extraction of the maximum number of Si-H bonds that can break at the interface, (b) K_F extraction example for a static stress condition, (c) K_F extraction results with corresponding linear fit leading to equation (14) for five stress conditions on a $0.09 \times 4.8 \mu\text{m}^2$ device and (d) K_R extraction results for the three DUTs leading to an Arrhenius law

modeling is reported in [12] along with its temperature dependence.

Therefore, the modified expression of K_F is presented in equation (14) as,

$$K_F = g_{rate} J_{AVL} \exp(\mu_F V_{CB}) \quad (14)$$

where g_{rate} is the fraction of the avalanche current density and μ_F is an exponential factor which governs the acceleration of hot-carriers due to the electric field.

The dependence of the trap generation is more significant on V_{CB} than on the J_{AVL} parameter. Indeed only a fraction (governed by the g_{rate} parameter) of the avalanche current density will reach the spacer interface while the hot-carriers will largely be accelerated by the electric field (through μ_F parameter) [6]. The use of J_{AVL}

instead of J_E simplifies the previous expression proposed in [8].

5.3. Trap annihilation rate

The second term of equation (6) corresponds to the trap annealing which depends on the number of hydrogen atoms available at the vicinity of the interface as well as on trap annihilation rate through K_R . The parameter extraction has been performed using the Levenberg-Marquardt optimization algorithm with fixed values of other model parameters (simulation conditions presented in figure 7d). The procedure has been repeated for different stress conditions and geometries leading to an

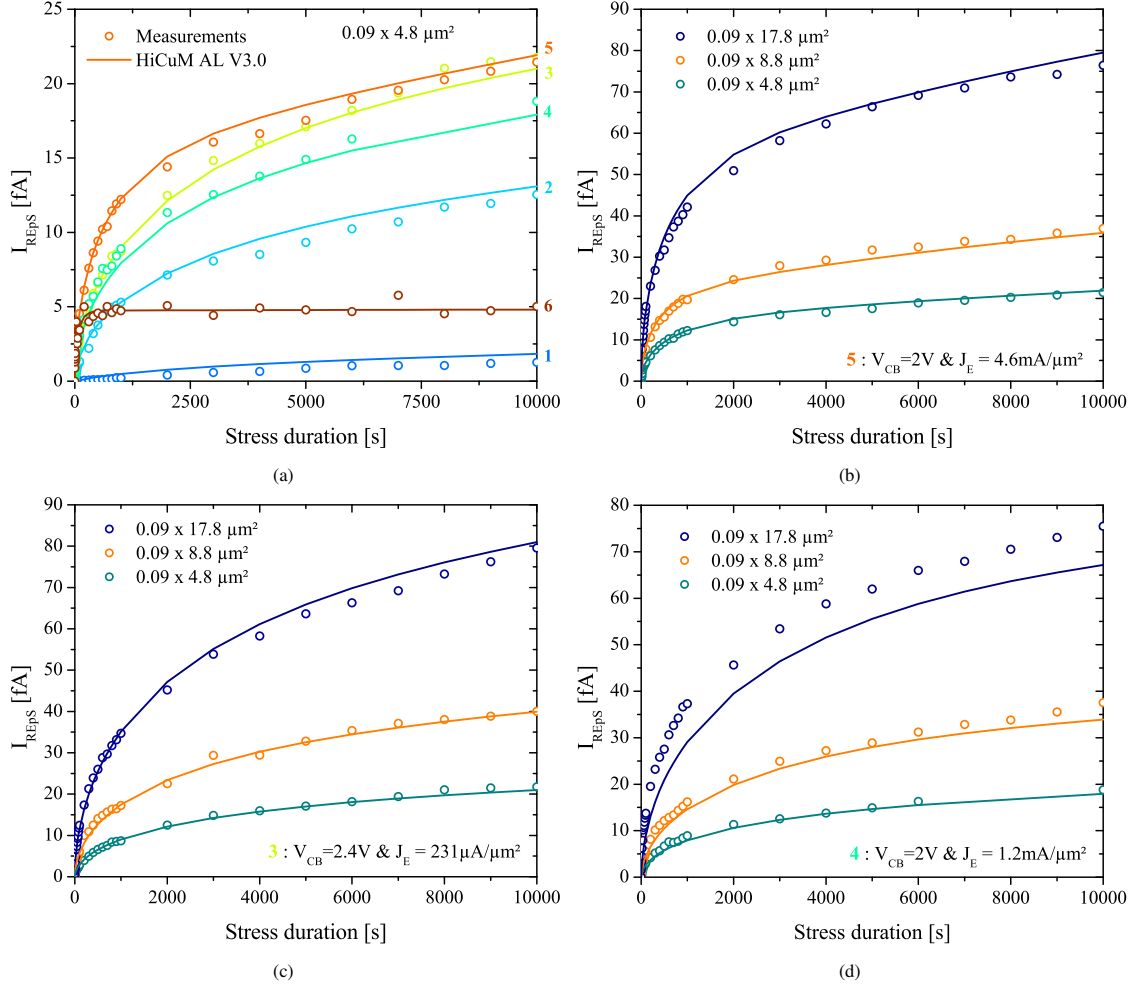


Figure 8: HiCuM-AL V3 simulations (lines) vs measurements (symbols) for (a) various aging tests (see table 2) on $0.09 \times 4.8 \mu\text{m}^2$ device and three static stress conditions in (b), (c) and (d) on all DUTs

Arrhenius law as expressed by equation (15).

$$K_R = K_{R0} \exp\left(-\frac{E_{aR}}{kT_j}\right) \quad (15)$$

where T_j is the device temperature calculated using HICUM thermal node [15].

6. Scalable aging compact model verification

The presented aging compact model (HiCuM AL V3.0) has first been validated on various stress conditions (see figure 5a) for a $0.09 \times 4.8 \mu\text{m}^2$ HBT device. The comparison between the measurements (symbols) and the simulations (lines) is presented figure 8a. Very good model accuracy is achieved for various operating conditions conforming to the scaled formulation for the

trap generation rate K_F and the temperature dependence of the annealing rate K_R . Interestingly, the stress condition at high junction temperature (brown curve in fig 8a) demonstrates a dynamic equilibrium between trap generation and annihilation which is well captured by the aging model.

Next, the model has been validated for different emitter dimensions with comparable stress conditions (e.g. same V_{CB} and J_{AVL}). A very good agreement is obtained between the measurements and the simulations for two stress conditions plotted in figure 8b and 8c. Some discrepancies are observed in figure 8d with slight under-estimations of the degradation for the two largest devices. The main explanation of these differences is that the initial value of the I_{REPS} parameter was larger than the values predicted by the model (due to the tech-

Parameters	α [A]	D_0 [$\mu\text{m}^2/\text{s}$]	E_a [eV]	μ_F [V^{-1}]	g_{rate} [$\mu\text{m}^2.\text{A}^{-1}.\text{s}^{-1}$]	K_{R0} [$\mu\text{m}^3/\text{s}$]	E_{aR} [eV]
Values	1.25×10^{-19}	4.64×10^{-1}	0.48	2.0	0.84	2.05	0.56

Table 4: Extracted model parameters for HiCuM AL V3.0 and a BiCMOS 55nm technology

nological variability between 2 dies) revealing a higher number of pre-existing traps before the beginning of aging tests. However, the scalable aging compact model demonstrates sufficient accuracy for various operating conditions and various emitter dimensions allowing its further exploitation in circuit reliability simulation.

The table 4 is provided as a summary of the extracted parameters for the scalable aging compact model formulation (HiCuM AL V3.0).

7. Conclusion

In this work, we have demonstrated that HCD depends on the spacer morphology. Indeed, increasing the degradation area at the interface increases the potential number of traps. Thus, a scalable formulation (HiCuM AL V3.0) has been proposed to enhance the former physics-based aging compact model. This new aging compact model is compatible with SiGe HBT architectures and dimensions. The aging compact model has been validated against aging tests on a 55nm BiCMOS technology confirming its accuracy against various stress conditions and geometry features. The scaled formulation can now easily be adapted for circuit simulations where scalable model cards are frequently used. Owing to its physical basis, the proposed model can provide accurate reliability predictions for circuits operating close to and beyond the SOA.

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