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Novel Quantum Dot Based Memories with Many Days of Storage Time

Last Steps towards the Holy Grail?

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***Abstract*— The feasibility of the QD-Flash concept, its fast write and erase times, is demonstrated together with storage times of 4 days at room temperature. The storage time of holes in (InGa)Sb QDs embedded in a (AlGa)P matrix can be extended by growth modifications to 10 y. Tunneling structures were recently demonstrated to solve the trade-off conflict between storage time and erase time. A QD-NVSRAM is suggested to become the first commercial application.**

Keywords-quantum dots, QD-flash, tunneling, NVSRA

I. INTRODUCTION

An important limitation of charge-based memories is the so called "voltage-time dilemma". The essence of this dilemma is to achieve 10 years in data retention by a barrier, that needs to be overcome during the write process. If typical barriers like pn-junctions in silicon or the conduction band offset of a dielectric like silicon dioxide to the silicon semiconductor are used, the consequence, is that a memory cell can either be nonvolatile or fast. In practical scenarios were dielectrics are used as barriers also the endurance will be limited for nonvolatile memories. This is the reason why there is such a huge performance gap between random access memories like DRAM or SRAM that are volatile and nonvolatile memories. QD Flash promises to solve this dilemma by using self-organized nanostructures in compound semiconductor systems, where the barrier height can be tuned much easier than in the systems used in silicon technology [1]. As a result, a memory cell that is both nonvolatile and possesses all attributes of a random-access memory (RAM) can be realized, meaning it will have a fast write speed and unlimited endurance. Such a memory cell would be ideal to complement or even replace DRAMs in the memory hierarchy and has been hailed more than 10 years ago as the "holy grail" of solid-state memories [2][3]. THIS "HOLY GRAIL" WOULD OFFER UNIQUE NEW FUNCTIONALITIES ENSURING FUTURE PROGRESS OF MEMORY DEVELOPMENT AFTER THE END OF MOORE'S LAW.

II. QD-FLASH: PRINCIPLE OF FUNCTION

QD-Flash is based on self-organized quantum dots (QDs) inserted in III–V compound semiconductor heterostructures. Using III–V materials allows for fine-tuning of the band offsets and barriers in the device, thus guaranteeing much greater flexibility than the Si/SiO_2 material combination. Furthermore, QDs eliminate the need for high electric fields, since capture of charge carriers occurs thermally in a fast and efficient fashion.

In a recent review [4], we presented the concept of the QD-Flash memory alongside with results obtained until 2016. The write time in QD-Flash is limited only by thermal capture into the QDs, which occurs in a few picoseconds at room temperature. The erase time depends on the localization energy of the QDs and on the external voltage applied. Appropriate tuning of these parameters can lower the erase time to tens of nanoseconds. The storage time depends on the localization energy and capture cross-section of the QDs. These parameters are determined by the choice of materials used to manufacture the heterostructure and the size of the QDs. Changing the heterostructures from GaAs-based ones to GaP-based ones, allowing growth on Si, and from type I to type II arrangement of the bands, thus increasing the confinement has led recently to an increase in the storage time from nanoseconds to 4 days at room temperature [5]. QDs in III–V heterostructures form a triangular barrier, the shape of which depends on the external voltage. As a consequence, its width can be changed at will, thus speeding up or slowing down the erase process. The triangular barrier also allows for much lower electric fields during the erase process, thus increasing the durability of the device. Finally, QDs in III–V semiconductors can be manufactured to store holes instead of electrons employing the type II band alignment. Since holes have a larger effective

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mass than electrons their storage time is much longer for the same localization energy.

III. QD-FLASH CELLs

A QD flash cell is a modulation-doped field effect transistor (MODFET), in which a layer of QDs has been embedded between the 2-dimensional hole gas (2DHG) and the gate. Fully functioning protypes have been manufactured already 8 years ago using InAs QDs embedded in GaAs or $Al_{0.9}Ga_{0.1}As$ [6], thus demonstrating the feasibility of the QD-Flash concept.

The charge state of the QDs is controlled by the gate voltage and read out is done using the 2DHG. The structure of QD-Flash is sketched in Fig. 1

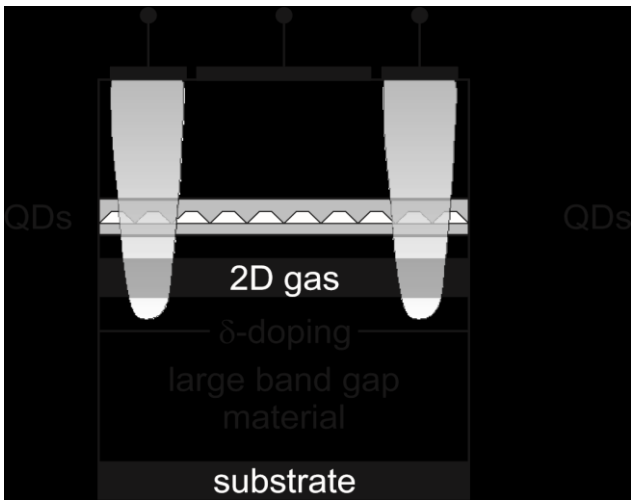


Fig. 1: Sketch of a QD-Flash

The logic state "0" is realized in a QD-Flash when the QDs are not occupied by holes. Conversely, the logic state "1" is realized when holes are localized in the QDs. The band structure configuration of QD-Flash during the basic operations (store, write and erase) is depicted in Fig. 2. In the storage configuration (Fig. 2a), if holes are confined (logic state "1") they cannot escape the QDs because of their huge localization energy, which thus represents the emission barrier. If the QDs are not charged (logic state "0"), the holes present in the valence band are prevented from entering the QDs by the triangular barrier created by the band-bending of the Schottky gate contact, which thus represents the capture barrier. The storage time of QD-Flash is determined by the capture and emission rates of the QDs [6]. In this system, capture and emission are dominated by thermally assisted tunneling. Consequently, the storage time depends on the barrier height, temperature and applied voltage. In order to write a logic "1", a write pulse is applied to the gate. The pulse is chosen to bring the system into flat band configuration (Fig.2b). The capture barrier is removed, and holes are thermally captured into the QDs.

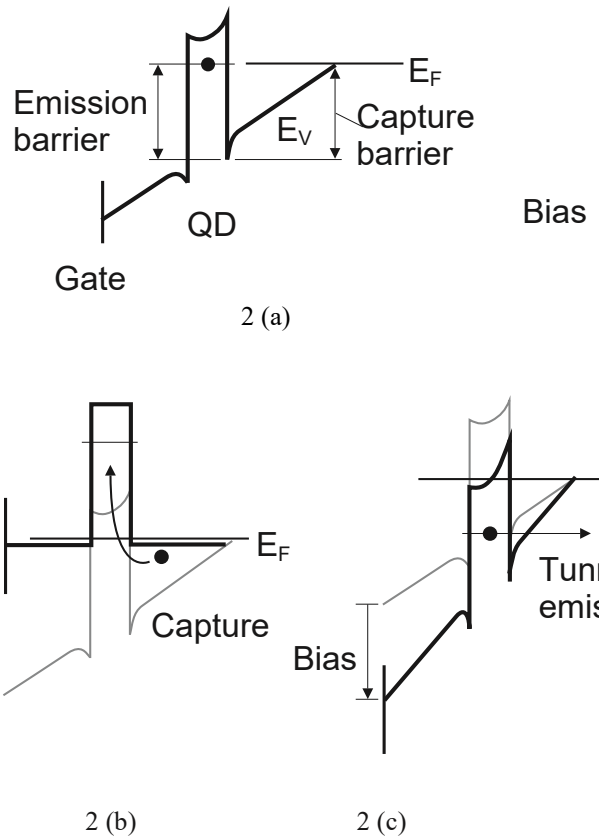


Fig.2: Schematic representation of the valence band during memory operations in QD-Flash: (a) store, (b) write (writing "1"), and (c) erase (writing "0").

Thermal capture is a very fast process, with time constants of the order of the picoseconds at room temperature [6].

Conversely, erasing (i.e. writing the logic "0") is performed by applying an opposite bias to the gate. The erase pulse bends the valence band even further, thus making the triangular barrier thinner (Fig. 2c). This in turn allows the charge carrier to tunnel out of the QDs, effectively erasing the stored data. Erase times much below 1 ns have been predicted with an appropriate choice of applied electric field and employing tunnel junctions [7].

Charge carriers are captured to the QDs from the 2DHG, which is therefore depleted whenever the QDs are charged.

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Moreover, confined charge carriers interfere with conduction in the 2DHG through Coulomb scattering. The combination of these two effects causes the conductivity of the 2DHG to fall when the QDs are occupied and to rise when they are unoccupied. Therefore, a simple measurement of the source–drain resistance serves as read-out of the storage state of the device.

IV. MATERIAL SCIENCE CHALLENGES

Much longer storage time are predicted for the GaSb/GaP system as compared to the InAs/GaAs QDs, due to larger hole localization energy in type II structures and the larger band gap discontinuity [1]. We have therefore investigated for the first time the quite challenging growth of GaSb QDs on (001) GaP substrates by means of Molecular Beam Epitaxy (MBE) [8]. QD growth was performed by deposition of 1.2 to 2 monolayers (ML) GaSb on GaP at a growth temperature ranging from 410 to 485°C and growth rates of 0.1 to 0.2 monolayers per second (ML/s). QD diameter, height and density have been systematically determined by atomic force microscopy and their dependence on the growth conditions has been interpreted in terms of scaling theory. Typical measured values lead to densities in the 10^{10}/cm^2 range, diameter around a few tenths of nm and height between 3 and 6 nm, which make these QDs valuable candidates for the targeted memory applications (Figure 3).

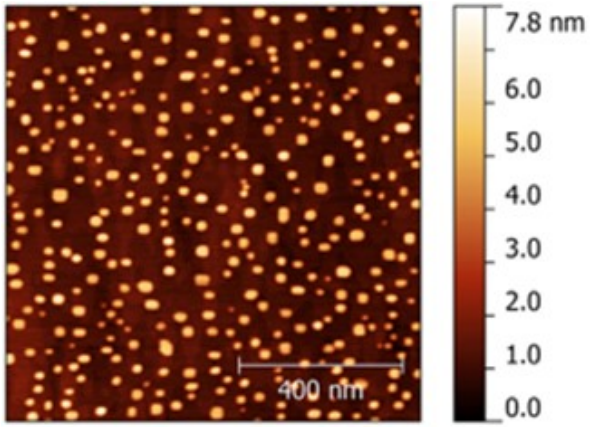


Fig. 3: 1µmx1µm AFM image of GaSb QDs after deposition of 1.2 ML GaSb on a (001) GaP surface at 450°C at a growth rate of 0.1 ML/s and with a Sb/Ga ratio of 2.5. The resulting density is around 2x10^{10}/cm^2.

Similar QD layers as that depicted in figure 3 have been capped starting with a 7 nm thick GaP layer grown at 430°C at 0.2 ML/s. Then the growth has been interrupted for 4 minutes to increase the growth rate to 1 ML/s for the rest of the 900 nm thick capping layer with a progressive increase of the growth temperature from 430°C to 600°C. TEM analysis demonstrates that, upon capping, the QD layer morphology is strongly modified by a strong P/Sb exchange reaction leading to the formation of a 10 nm thick intermixed GaP/GaSb layers. In spite of the large mismatch between GaSb and GaP (11.8%), the QD layers are coherently grown on the substrates without any dislocations. Finally QD layers have been embedded in GaP and n $^+$ p- diodes have been fabricated. The localization energy, capture cross-section, and storage time of holes in the ground state of the quantum dots have been determined via deep-level transient spectroscopy. Their localization energy of 1.18(+/-0.01) eV agrees with the theoretical prediction of 1.4 eV once the observed interdiffusion is considered. As storage time of holes of 3.9 (+/-0.3) days at room temperature is determined, marking an improvement of 3 orders of magnitude from previous record numbers, see Fig. 4.

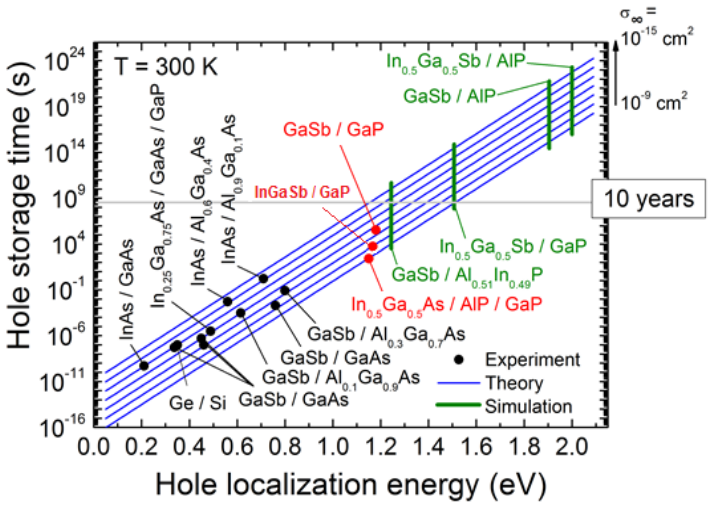


Fig. 4: Carrier storage time versus hole localization energy as a function of capture cross section.

Replacing the GaP barriers either by AlP or InAlP using either MBE or MOCVD will shift the hole storage time much beyond the 10y limit defined for Flash memories. Hole localization energies of 1.9.eV and 2.0 eV are expected for the material combinations GaSb/AlP and In0.5Ga0.5Sb/AlP, respectively, leading to hole lifetimes 10 orders of magnitude larger than presently observed [4].

V. OUTLOOK

Next material science work will focus on

- demonstrating the beyond 10 y lifetime for AlP/ or InAlP/InGaSb QDs,
- combining the tunnel junctions with the AlP/GaSb
- fabricate a GaP-based fully operational flash cell similar to Fig. 1 and

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- employ previously developed concepts [8] for single q-bit emitters for localising precisely QDs, targeting single QD memories

- start circuit design work for integration. A memory is more than 1 cell.

Thus in a few years' time Si-compatible quantum dot memories could catch the NVSRAM market. In the long run it could even become the non-volatile alternative for today´s DRAM technology the industry has been seeking for more than two decades now. .

References

[1] D. Bimberg et al., *Memory*, U.S. Patent N. 8331142 B2, December 2012 and other US and EU patents.

[2] M. Inman, New Scientist, Daily News, March 7, 2008

[3] T. Mikolajick, C.-U. Pinnow, Proceedings of NVMTS, p. 4-6 (2002)

[4] D. Bimberg and L. Bonato, "QD-Flash: Towards non-volatoility in quantum dot based storage", Proc. 24th Int. Symp. "Nanostructures: Physics and Technology", St. Petersburg Academic University, p.1, 2016

[5] L. Bonato Appl. Phys. Lett. 106,042102, 2015 and phys. stat. sol. (b) 253, 1871, 2016, and E.M.Sala et al., phys. stat. sol. (b) 255,1800182, 2018

[6] A. Marent et al., Semicond. Sci. and Technol. 26, 014026, 2011

[7] F. I. Arikan et al., phys. stat. sol. (a) 215, 180018, 2018

[8] L. Desplanque et al., Nanotechnology **28**, 225601 (2017)

[9] W. Unrau and D.Bimberg, Lasers and Photonics Review 8, 276, 2014

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