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Design of On-wafer TRL Calibration Kit for InP technologies characterization up to 500 GHz

Marina Deng, *Member, IEEE,* Chhandak Mukherjee, Chandan Yadav, *Member, IEEE,* Sébastien Fregonese, Thomas Zimmer, *Senior Member, IEEE*, Magali De Matos, Wei Quan, Akshay Mahadev Arabhavi, Colombo R. Bolognesi, *Fellow, IEEE*, Xin Wen, Mathieu Luisier, Christian Raya, Bertrand Ardouin and Cristell Maneux

***Abstract*—This paper reports a detailed approach towards optimization of on-wafer TRL calibration structures for sub-millimeter-wave characterization of a state-of-the-art InP technology, validated by thorough experimentation and electro-magnetic (EM) simulation. The limitations of the existing RF test structures for high frequency measurements beyond 110 GHz are analyzed through EM simulation. Using an optimization procedure based on calibration of raw EM simulated data, on-wafer TRL calibration structures were developed and fabricated in a subsequent run of this technology. Measurements could be achieved up to 500 GHz on the passive devices and up to 330 GHz on the InP DHBTs. The transistor measurements were validated by comparison with the HiCuM compact model simulation to 330 GHz for the InP DHBTs.**

***Index Terms*— characterization, compact model heterojunction bipolar transistor, electromagnetic simulation high frequency, indium-phosphide, sub-millimeter wave, terahertz**

I. Introduction

THE continuous improvement in RF performances of the Indium-Phosphide (InP) double heterojunction bipolar transistors (DHBT) has rendered this technology as an ideal choice for enabling terahertz (THz) circuit design as well as monolithic integration of electronic and photonic devices for optical or wireless link communication systems [1]-[2]. With cut-off frequencies ranging between 300 GHz and 1 THz [3]-[8] and breakdown voltages exceeding 4.6 V [3][6][8], the resulting excellent power handling capabilities at high frequencies allows the design of power amplifiers up to 600 GHz and 670 GHz [9]-[10].

However, the accurate characterization of sub-millimeter-wave devices beyond 110 GHz is particularly critical, as discussed in [11] and [12], as the limitations of calibration and de-embedding techniques and the difficulties of on-wafer measurements at high frequency are increased. Among the characterization works reported for InP DHBTs, the S-parameter measurements are usually performed below 110 GHz, using conventional calibration methods such as Short-Open-Load-Thru (SOLT) [7] or Line-Reflect-Reflect-Match (LRRM) [5][6] on commercial calibration substrates on alumina followed by an Open-Short or Short-Open de-embedding step. Beyond 67 GHz, on-wafer Thru-Reflect-Line (TRL) calibration kits have been developed, using conventional [4][13] or inverted [14][15] thin film microstrip (TFMS) transmission lines. In fact, at millimeter and sub-millimeter-wave frequency ranges, on-wafer calibration techniques, well known to outperform conventional calibration methods on alumina substrates [21], become indispensable to achieve accurate measurements for f_T/f_{max} assessment as well as transistor compact model verification for circuit design purposes. Besides, the TRL calibration does not require a perfect definition of the standards, contrary to the SOLT: only the thru and line delays are necessary and the reflect standard must be symmetrical. Owing to this on-wafer calibration approach, transistor's small-signal current and Mason unilateral gains could be computed from S-parameter measurements up to 110 GHz as reported in [4] and up to 750 GHz in [13], and model verification was performed up to 325 GHz [14][15].

In this paper, we propose optimized test structures of the InP DHBT technology from ETH-Zurich Millimeter-Wave Electronics Laboratory [6] in order to push the transistor characterization up to 330 GHz, thus enabling the verification of the f_T and f_{max} extrapolation as well as the transistor HICUM compact model simulation results [7]. An on-wafer TRL calibration kit was designed using coplanar waveguide lines in order to fully benefit from the state-of-the-art InP DHBT process, which, unlike silicon processes [16][17], does not provide a ground plane at the bottom metal layer. Previous works using coplanar waveguide (CPW) and grounded coplanar waveguide (CPWG) line standards for on-silicon TRL calibration have been reported up to 110 GHz [18] and 325 GHz [19][20], demonstrating the capability of this line topology to address on-wafer millimeter and sub-millimeter-

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M. Deng, C. Mukherjee, M. De Matos, S. Fregonese, T. Zimmer and C. Maneux are currently with IMS laboratory, University of Bordeaux, France (e-mail: marina.deng@ims-bordeaux.fr).

C. Yadav was with the IMS Laboratory, University of Bordeaux, France. He is now with the National Institute of Technology, Calicut, Kerala, India.

W. Quan, A. Arabhavi, C. R. Bolognesi, X. Wen and Mathieu Luisier are with the Department of Information Technology and Electrical Engineering, ETH Zurich, 8092 Zürich, Switzerland (e-mail: bolognesi@mwe.ee.ethz.ch).

B. Ardouin and C. Raya are with SERMA Technologs, Pessac, France.

wave measurements. The rest of this paper is organized as follows: section II presents an analysis of the limitations of the initial test structures (Generation 0, *i.e.* G0) for millimeter and sub-millimeter-wave measurements and suggests the design of optimized test structures (Generation 1, *i.e.* G1), including the implementation of test-structures for an on-wafer TRL calibration kit using coplanar waveguide transmission lines. In section III, the on-wafer TRL calibration kit was employed to characterize the InP DHBT technology up to 330 GHz and some proposals are provided to further enhance the test structure design by using predictions from EM simulation in order to improve the measurement accuracy for reliable transistor characterization up to 500 GHz.

II. Test Structure Layout Improvements

A. G0 preliminary results up to 220 GHz

In order to get insights into the layout design limitations, the first generation (G0) of RF test structures for InP DHBT characterization was measured from DC to 110 GHz and from 140 to 220 GHz. The S-parameter measurements were carried out up to 110 GHz using an Agilent® E8361 PNA, with frequency extenders for the 67-110 GHz frequency range, and in the *G*-band (140–220 GHz) using a Rohde & Schwarz® ZVA24, coupled with Rohde & Schwarz® frequency extenders. The pad layout allowed a minimum probing pitch of 100 µm. Hence, Picoprobe® probes were used in the 1–110 GHz and Cascade Infinity® probes were used in the *G*-band, both with 100 µm probing pitches. In each frequency range, an off-wafer SOLT calibration was performed with the probe-paired commercial calibration substrate, Picoprobe CS-15 and Cascade 138-357 calibration kits. The off-wafer SOLT calibration is known to provide inaccurate calibration at very high frequency due the lumped element equivalent circuits that describe each standard. Indeed, with the increase of frequency, distributed effects can occur, which are not taken into account in such lumped models. However, this full two-port calibration method offers the advantages to be compatible with any probe design, as opposed to LRRM that is best suited to Cascade probes, and also takes into account the crosstalk between ports, which is not the case in the 8-term error models of LRRM and TRL. A previous work carried out for SiGe HBT [21] showed a clear limitation of SOLT above 200 GHz due to the probe-to-substrate coupling, difference between the calibration standards on alumina and the on-wafer test structures measurements, as well as distributed effects rising at these high frequencies. But below 200 GHz, for these scaled on-wafer test structures, the off-wafer SOLT and on-wafer TRL produced comparable results. Hence, a common SOLT calibration method was chosen for G0 measurements for both frequency ranges, even though we were aware of the SOLT limitations at the upper range of the *G*-band.

The G0 test structures consisted of a transistor and its corresponding open and short test structures for de-embedding (Fig. 1). The pad is 150 µm long and 40 µm wide.



a) b)

Fig. 1. G0 test structures' layout: a) transistor's open; b) transistor's short

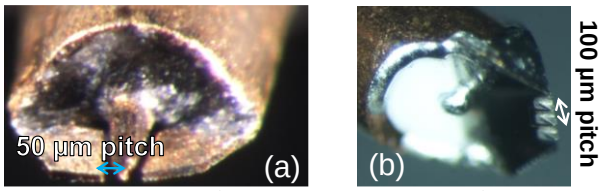


Fig. 2. Optical images of Picoprobe (a) and Cascade Infinity probes (b)

During measurement, the Picoprobe and Infinity probes require a different overtravel due to a different design. Indeed, these probes present a totally different design, as depicted in Fig. 2: CPW type for Picoprobe and microstrip type for Cascade Infinity. Also, larger trace and larger overtravel are necessary for Picoprobe probes to make a good contact on the RF Ground-Signal-Ground pads. Moreover, the small thickness of the gold deposition forming the pads does not allow several contacts on the same position. In view of these constraints, using different probes in the two frequency ranges 1–110 GHz and the *G*-band obviously led to a different probe tips' positioning. The resulting measurements show band discontinuities, as observed in the measured Open capacitances and Short inductances depicted in Fig. 3 and Fig. 4, respectively. Furthermore, a different probe-to-substrate interaction due to these dissimilar probes' design, amplified by the probe-tip calibration transfer from alumina to InP substrate is certainly another reason that can explain the band discontinuities.

To study the positioning impact, the 3D EM simulation procedure using Ansys® High-Frequency Structure Simulator (HFSS) to simulate the SOLT calibration on alumina substrate, described in [21], was used. Two positions of the probe tips were considered. As done in [21], the layout of the Open and Short test structures was imported into HFSS (see insets of Fig. 3 and Fig. 4). The layer description was set according to the epitaxy of the ETHZ InP technology, considering a gold layer deposited on a Teflon layer on top of the InP substrate forming the test structures. The EM simulation could reproduce the measurements' trend when considering a contact at the pad outer-edge (1-110 GHz) and at the pad center (140-220 GHz). Below 110 GHz, the positioning impact leads to 1-2 fF capacitance difference on the Open measurement (10%) and 10 pH inductance difference on the Short measurement (20%). The deviations become even greater with increasing frequency, worsening the band discontinuity. This confirms the high sensitivity of the probe positioning when using SOLT calibrations on alumina substrate for successive measurement frequency bands.

Moreover, in both measurement and EM simulation, a resonance (strong increase) at 200 GHz is observed on the

Open's capacitances and Short's inductances (see Fig. 3 and Fig. 4). Since these test structures cannot be modelled by ideal capacitances and inductances, as a consequence, they cannot be used for the Open-Short de-embedding of the transistor's accesses. This comes from the inappropriate pad length for measurements beyond 140 GHz. By reducing the pad dimensions, we expect to push the resonance of the Short's inductances further towards higher frequencies, so that the lumped model of the Open and Short test structures respectively provides a constant capacitances and inductances beyond 140 GHz.

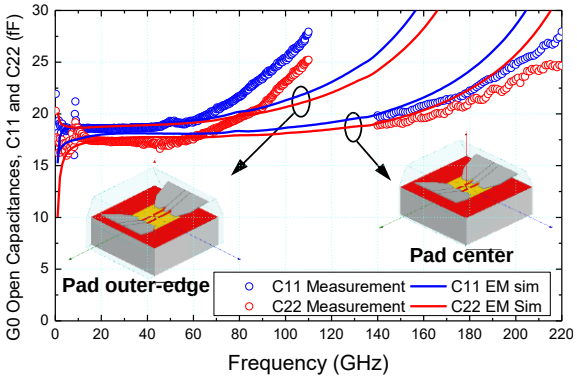


Fig. 3. Measured and simulated G0 transistor's open capacitances up to 220 GHz.

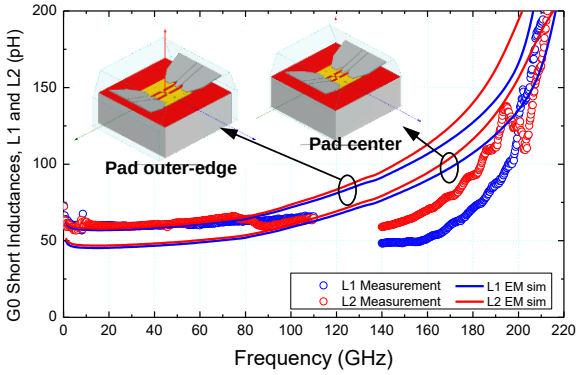


Fig. 4. Measured and simulated G0 transistor's short inductances up to 220 GHz.

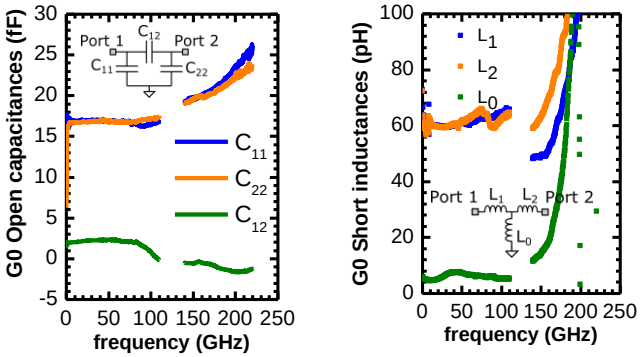


Fig. 5. G0 Open capacitances (a) and Short inductances (b): measurements up to 220 GHz after probe tips positioning correction (pad's outer edge).

Finally, pristine G0 open and short structures were measured by carefully positioning the probe tips in the same place from 1 to 220 GHz (see Figs. 3 and 4). The new measurements demonstrated a better band continuity for the Open structure as observed in Fig. 5.

B. G1 layout improvements

1) Pad layout design

As observed in the previous section, the G0 test structures demonstrated rather high values of pad inductances which make de-embedding of the transistor's accesses with passive test structures unreliable at frequencies beyond 110 GHz. Thus, to reduce the effect of the pad parasitics, the pad layout of the first generation (G0) has been modified leading to the new generation of test structures, G1. Also the new signal pad size was reduced to 60×30 µm² (50% laterally and 25% vertically) with 50 and 100 µm probing pitch compatibility. Furthermore, in order to better confine the RF signal and thus optimize its propagation along the access line, we connected the north and south ground pads surrounding the signal pads (see Fig. 6) as suggested in [21]. The reduction of the access length helps to extend the validity range of a lumped based de-embedding method, such as Open-Short or Short-Open, since the resulting capacitance and inductance would remain constant up to millimeter-wave frequencies. The transistor's open and short characterization will be presented in the next section.

The test structures have a pad metal of 910 nm thickness deposited on the 800 nm Teflon layer on top of the 350 µm InP substrate. In order to get a 50 Ω characteristic impedance for the CPW access line forming the pad using the composition of this layer, the layout of the new pad includes a gap between the ground and signal pads of 15 µm. This also allowed the use of 50 µm-pitch probes for characterization at frequencies higher than 110 GHz, which are preferable for lower insertion loss and are better scaled for millimeter and sub-millimeter-wave on-wafer measurements.

2) On-wafer TRL calibration kit development

To ensure more reliable calibration up to 500 GHz, on-wafer Thru-Reflect-Line (TRL) calibration test structures have been designed for the G1 generation (Fig. 6). The on-wafer TRL calibration kit includes a 60 µm Thru, a Pad-Open as reflect and two lines covering the frequency range from 35 to 500 GHz: 180 µm Line_300G (35-316 GHz) and 120 µm Line_600G (70-633 GHz).

Considering as first approximation the relative permittivity of the InP substrate which thickness is preponderant compared to the Teflon layer's one, the frequency range (f_{min}, f_{max}) of each line was calculated using the following equations [24]:

$$f_{min} = \frac{c_0}{20\times\sqrt{\varepsilon_r}\times(l_{LINE}-l_{THRU})} \quad (1)$$

$$f_{max} = \frac{9\times c_0}{20\times\sqrt{\varepsilon_r}\times(l_{LINE}-l_{THRU})} \quad (2)$$

with c_0=3×10^8 m/s and $\varepsilon_{r,\,InP}$=12,6

After on-wafer TRL calibration, the reference plane is set at the inner edge of the Pad-Open as shown in Fig. 6-b.

In the floor plan of the G1 layout, all the test structures were placed with a vertical distance of 140 µm and a horizontal

distance of 80 µm minimum between them.

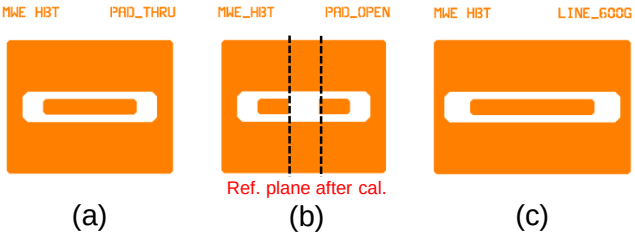


Fig. 6. G1 on-wafer TRL calibration kit standards: a) Thru, b) Pad-Open (reflect), c) Line 600G (for 70-633 GHz calibration).

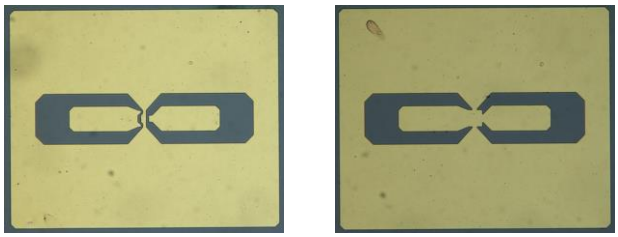


Fig. 7. G1 test structures' layout: a) transistor's open; b) transistor's short

III. InP DEVICES CHARACTERIZATION UP TO 500 GHz

A. *Passive devices characterization up to 500 GHz*

As presented in Fig. 7, the G1 transistor's open and short design both benefited from the pad size reduction. After TRL calibration using the developed on-wafer calibration kit presented in the previous section, their S-parameters were measured from 500 MHz to 500 GHz, by the means of four frequency band measurements: 500 MHz to 110 GHz, 140 to 220 GHz, 220 to 330 GHz and 325 to 500 GHz (the two last setups consist of the Rohde & Schwarz ZVA24 coupled with extenders as the *G*-band setup). Picoprobe RF probes with 100 µm pitch were used up to 110 GHz, then Picoprobe RF probes with 50 µm pitch were used between 140 and 500 GHz.

Fig. 7 and 8 compare the transistor's open capacitances and transistor's short inductances extracted from the S-parameter measurements from the two generations of test structures. These two de-embedding test structures are quasi-symmetrical in both G0 and G1, which is why only one-port capacitance or inductance is showed in Fig. 8 and Fig. 9. By comparing measurements of G0 (after SOLT calibration on alumina substrate at probe tips up to 220 GHz) and G1 (after on-wafer TRL calibration at pad's inner edge up to 500 GHz) test structures, a very significant lowering of about 10 fF in the C_{11}/C_{22} open capacitances and of 50 pH in the L_1/L_2 short inductances is observed for the new test structures (G1). Moreover, the pad capacitances of G1 exhibit rather flat frequency responses up to 500 GHz, compared to that of G0. This major improvement obviously justified the need for a better test structure scaling with a pad size reduction and an on-wafer TRL calibration kit design suitable for millimeter-wave measurements.

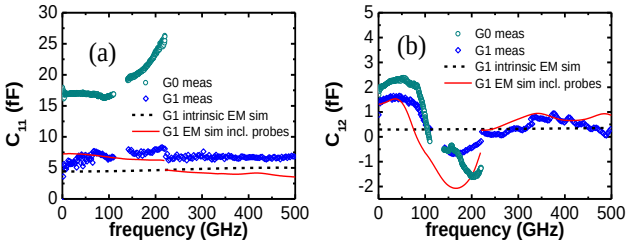


Fig. 8. G0 and G1 transistor's open capacitances extracted from measurements (symbols) and EM simulation (lines) up to 500 GHz: a) port-1 capacitance C_{11} (quasi-symmetrical open), b) port-1 to port-2 capacitance C_{12}

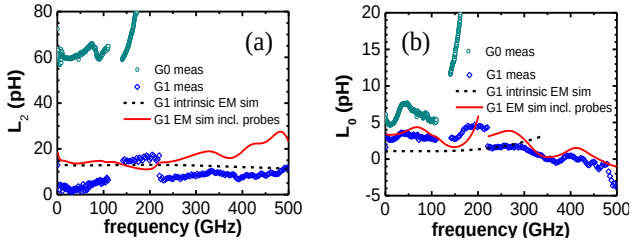


Fig. 9. G0 and G1 transistor's short inductances extracted from measurements and EM simulation up to 500 GHz: a) inductance L_2 on output access (symmetrical short), b) inductance L_0 on ground access

The EM simulations corresponding to the G1 structures are also shown in Fig. 8 and Fig. 9, providing a physical trend for the measurements. Two sets of EM simulations are presented: i) EM simulation of the intrinsic device under test (DUT) without RF pad (black dashed lines), at the reference plane of the TRL calibration as depicted in Fig. 6-b; ii) EM simulation of the complete DUT and TRL calibration standards including RF pads, RF probes and neighbors (red lines), following the methodology described in [17] for the TRL calibration of raw EM simulated data. The intrinsic EM simulation stands for the reference behavior, while the complete EM simulation with pads and probes shows additional effects due to the measurement setup and the calibration method. Particularly, in order to reproduce the complete measurement setup by EM simulation, a specific model of the RF probes of each frequency band, with the corresponding probing pitch, as well as neighboring structures, has been taken into account in the HFSS EM simulator [25], as along with the real probe positioning during measurement and the electrical coupling between the adjacent structures. The comparison is also drawn between measured and simulated S-parameters of these two devices in Fig. 10 and Fig. 11at the same reference plane as the measurements. Again, a good reproduction of the measured S-parameter magnitudes and phases by the complete EM simulation guarantees an accurate and reliable characterization of the transistor open and short up to 500 GHz. Interestingly, the magnitude of S_{11} and S_{22} for the open structure (Fig. 10-(a) and (c)) shows an increase above 0 dB, especially in the 250-300 GHz range, which the full EM simulation also reproduces. This is likely due to the EM coupling between the neighboring structures and crosstalk between port 1 and port 2, since the intrinsic EM simulation does not show such effects.

To investigate this further, we have considered two

scenarios in EM simulation depicted in Fig. 12 for the open structure. The first one represents the G1 design, where in the gold layer upon the Teflon layer is etched in order to reveal each individual test structure. The second scenario is where the gold layer upon the Teflon layer is not etched around the test structures so that the ground pads are all connected together creating a "continuous ground plane" for the entire chip. In Fig. 12-b, the electric field (E-field) distribution computed by EM simulation at 150 GHz clearly shows a coupling between the neighbouring structures and to a lesser extent, a coupling between ports (crosstalk). For the second scenario, the E-field distribution indicates a strong reduction of the coupling between the neighboring structures. This

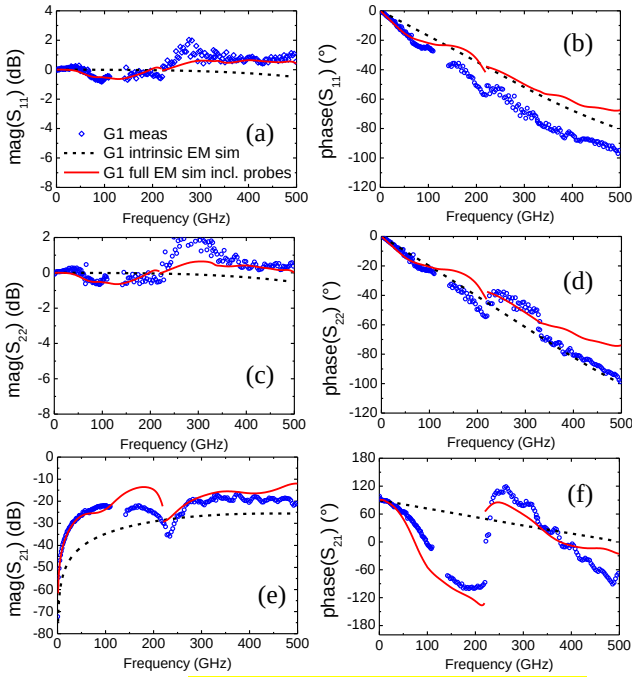


Fig. 10. S-parameters in magnitude (a),(c),(e) and phase (b),(d),(f) of the transistor open structures comparing the measurement (symbol) and the EM simulation (dashed line=intrinsic device simulation, straight line=complete device simulation including RF pads and probes + TRL calibration)

second scenario can thus be the solution adopted for the next generation of InP devices, G2, in order to further improve the accurate characterization of InP based devices.

Another reason behind the apparition of distributed effects at higher frequencies could be the parasitic modes in CPW [22] such as the slot line mode, microstrip mode and eventually surface wave parallel-plate modes in the substrate. Two options can be proposed to reduce the impact of these parasitic modes:

i. the first one is based on a proper scaling of the CPW line by reducing the width and the gap. Preliminary EM studies show that reducing the width of the CPW down to 15µm would help to reduce some of the parasitic modes [26]. Still, one should also cancel the slot line mode by keeping the same potential on the ground plane with considering the short wavelength at such high frequency;

ii. the second option would be to modify the back-end of the line as suggested by Urteaga [4] and Williams [13], particularly by adding a benzocyclobutene (BCB) dielectric having superior dielectric properties and using a microstrip line topology.

Nevertheless, the main improvement of the G1 test structures is the use of such scaled open and short test structures for accurate de-embedding of the transistor's access up to 500 GHz.

B. InP DHBT characterization up to 330 GHz

The transistor under test from G1 generation, with an emitter width of 0.2 µm and an emitter length of 10 µm, was fabricated following the process described in [6]. The InP DHBT was biased at different base-emitter voltages from 751

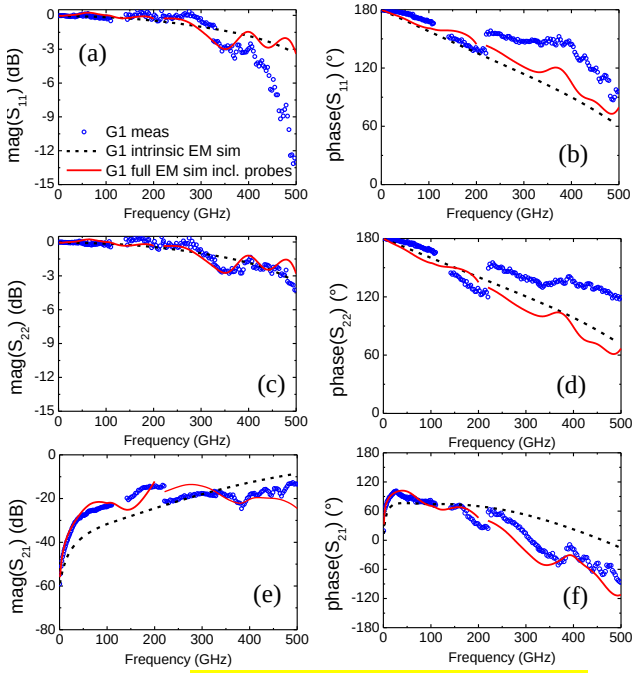


Fig. 11. S-parameters in magnitude (a),(c),(e) and phase (b),(d),(f) of the transistor short structures comparing the measurement (symbol) and the EM simulation (dashed line=intrinsic device simulation, straight line=complete device simulation including RF pads and probes + TRL calibration).

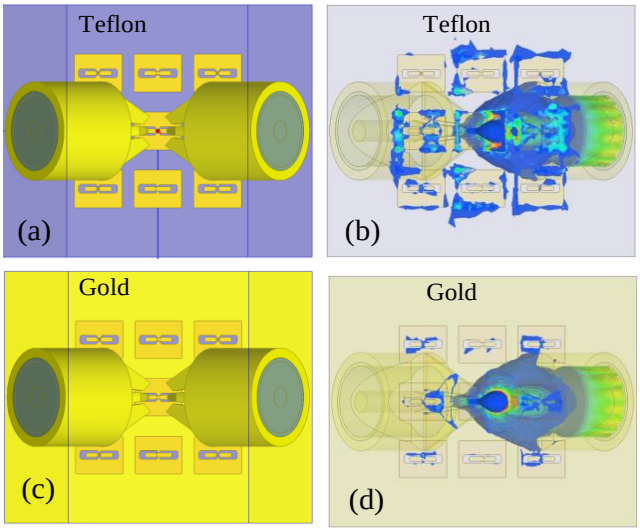


Fig. 12. EM simulation configurations and the corresponding E-field distribution at 150 GHz (bottom views): a)-b) for G1 with Teflon as dielectric around test structures; c)-d) for G2 with gold layer, upon Teflon, creating a continuous ground plane around all the test structures

mV to 853 mV by 34-mV step, while keeping the collector-emitter voltage constant at 1 V. The S-parameters were measured from 0.5 to 110 GHz, from 140 to 220 GHz and finally from 220 to 330 GHz using the same setups described in section II.

The on-wafer TRL calibration was performed using the measurements of the developed calibration kit (see section II), setting the reference plane along the access line, at the edge of the Pad-Open. A Short-Open de-embedding step was then used to bring the reference plane at the intrinsic transistor's terminals in order to allow comparison with the HiCuM compact model simulation corresponding to this transistor's geometry. The scalable HiCuM model parameters were extracted for different G1 transistor geometries following the same procedure used for G0 transistors in [7]. In Fig. 13, the measured and simulated S-parameters are shown for the applied bias depicting 500/700 GHz peak f_T/f_{max} for a 0.25×10 µm² InP DHBT, at V_{BE}=853 mV, V_{CE}=1V (a decrease of the collector current from 30.3 to 26.3 mA was observed over the three frequency bands measured up to 330 GHz). Regarding the S-parameter magnitudes, the deviation between measurement and simulation stays below 1.4 dB up to 110 GHz and, except for $|S_{12}|$, the maximum deviation between 140 and 330 GHz is 6 dB. As for $|S_{12}|$, we suspect this to be the results of crosstalk, due to coupling between port 1 and port 2, as previously observed on the open measurements and confirmed by EM simulation. One solution that could be considered to prevent crosstalk in the design of next generation G2 test structures would be to extend the Thru length to 100 µm. Concerning the S-parameters phases, the deviation between measurement and simulation is at most 10° for S_{12} and S_{21}, but a slightly larger deviation for the S_{11} and S_{22} parameters is observed. Considering both the magnitude and phase of the S-parameters, satisfactory agreement between HiCuM compact model and measurements up to 330 GHz can be observed for most of the S-parameters that has never been demonstrated so far.

Since f_T and f_{max} are key figures of merit to demonstrate the RF performances of this InP DHBT technology, we computed, from both measurement and simulation, the current gain, H_{21}, and the unilateral Mason gain, U, in order to be able to extrapolate f_T and f_{max} versus frequency, as depicted in Fig. 14 and Fig. 15, respectively, for different bias conditions of the transistor under test. Here also, the HiCuM compact model is consistent with the measurements, thereby providing a reliable RF behavior prediction of the InP DHBT up to 220 GHz. In fact, the measurements of the transistor are also affected by the crosstalk observed for the passive devices, which deteriorates f_{max} (well known to be highly sensitive to measurement imperfections) beyond 220 GHz. Moreover, the resonance observed near 150 GHz has been identified as the result of inappropriate Picoprobe RF probe design in the *G*-band.

Although G1 test structure optimization significantly improved the high-frequency characterization of the InP DHBTs compared to G0, further improvement will be enabled by additional layout enhancement. Particularly, to access the intrinsic transistor behavior beyond 220 GHz through all S-parameters, improved calibration standards need to be designed by taking into account the neighboring effects and crosstalk. As indicated above, electromagnetic simulation can be efficiently used to provide solutions to reduce coupling between neighboring structures at higher frequencies.

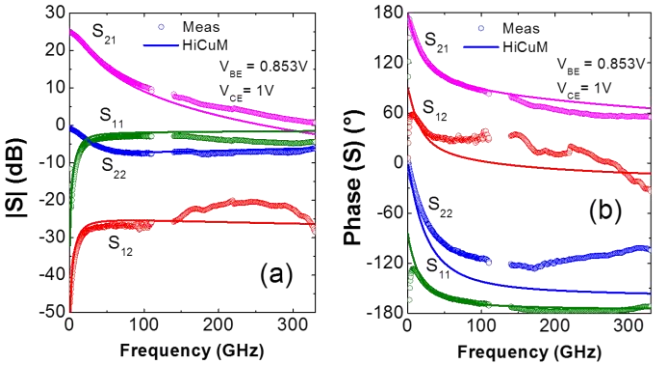


Fig. 13. Measured and simulated S-parameters of the InP HBT up to 330 GHz: a) magnitude; b) phase

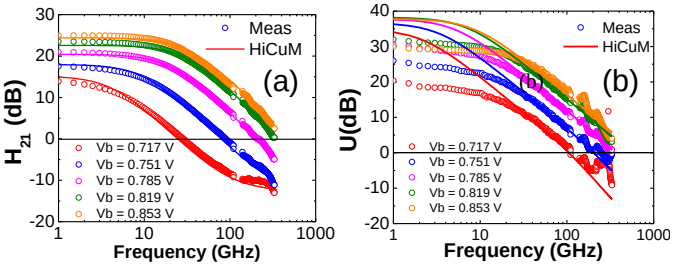


Fig. 14. Measured and simulated gain curves of the InP HBT up to 330 GHz: a) $|H_{21}|$ current gain; b) |U| Mason gain

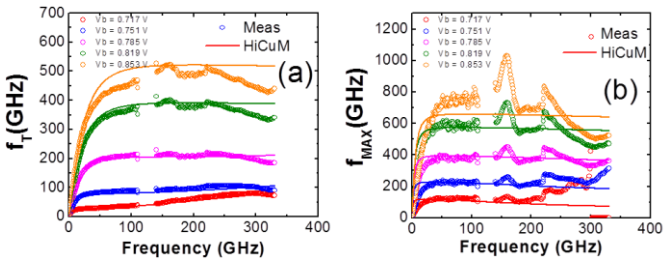


Fig. 15. f_T and f_{max} extrapolation versus frequency of the InP HBT up to 330 GHz: a) transit frequency f_T; b) maximum oscillation frequency f_{max}.

IV. Conclusion

In this paper we propose improvements of test structures for the characterization of InP devices up to 500 GHz using an optimization procedure based on EM simulation of calibration structures. By highlighting the limitations of test structure design validated by measurements and EM simulation of a previous technology generation up to 220 GHz, an improved pad layout design was proposed with optimized dimensions, along with the development of an on-wafer TRL calibration kit based on CPW transmission lines. Then, we demonstrated the validity of this calibration approach, for the first time using CPW lines, for passive devices' (open, short) measurement on InP substrate up to 500 GHz. As for the InP DHBT, we successfully demonstrated reliable transistor characterization and compact modelling using HiCuM model up to 330 GHz, despite some measurement uncertainties observed on f_{max} beyond 220 GHz. Further layout improvements aiming to reduce crosstalk and coupling between neighboring structures were proposed through EM simulation in order to extend reliable characterization of the InP DHBTs up to 500 GHz.

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