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Hugo Dewitte, Serena Rizzolo, Philippe Paillet, Pierre Magnan, Alexandre Le Roch, et al.. Annealing effects on Radiation Hardened CMOS Image Sensors Exposed to Ultra High Total Ionizing Doses. IEEE Transactions on Nuclear Science, 2020, 67 (7), pp.1284-1292. 10.1109/TNS.2020.3001618 . hal-03192270

HAL Id: hal-03192270
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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2020.3001618, IEEE Transactions on Nuclear Science

Annealing Effects on Radiation Hardened CMOS Image Sensors Exposed to Ultra High Total Ionizing Doses

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***Abstract*—Capabilities of rad-hard electronics are often degraded by post-irradiation annealing, whose effects need to be considered in designing complex systems, such as CMOS image sensors. In particular, the commonly accepted behavior of annealing cannot be systematically assumed, because reverse annealing does not necessarily come from the degradation of the defects, but could be the result of defects annealing non-uniformities. This paper provides an extensive study of the dark current and pixel readout electronic behavior of CMOS image sensors during irradiation and annealing, in order to provide some insights on these annealing non-uniformities. The isochronal annealing performed up to 300°C demonstrates that, up until a certain temperature, reverse annealing is almost always present, but the 300°C annealing always heals the system very efficiently. When performed on specially designed gated pixels for ultra-high dose applications, adding a N+ drain further mitigates the radiation effects along with the reverse annealing. This proves the efficiency of these rad-hard designs and calls for further research in this radiation hardening direction.**

I. Introduction

THERE is a growing demand for radiation-hard CMOS Image Sensors (CIS) that can be used in highly radiative environments – i.e. which are able to provide good quality and reliable images after very high dose absorption (higher than 1 MGy/100 Mrad(SiO_2)). This is especially true for nuclear applications, where the availability of such rad-hard CIS would permit easier, safer and more efficient operations, including the remote maintenance, monitoring and inspection of radioactive places that are not (or hardly) accessible by humans, such as nuclear power plant reactors, nuclear waste repository, experimental reactor (ITER) and next generation particle physics facilities (CERN, HL-LHC, LLNL National Ignition Facility, CEA Laser MegaJoule). This technology could also be beneficial to space endeavors that aim to explore the most radiative places of our Solar system: rad-hard electronics and CIS would allow to reduce the shielding needs – which represents a significant limiting mass – and produce higher quality images while extending the lifetime of the mission.

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Radiation Hardened By Design (RHBD) CIS are currently extensively studied [1] [2], most efforts being concentrated in reducing as much as possible their post-irradiation degradation. In that context, the annealing effect, when considered, is almost systematically assumed to improve the CIS post-irradiation performance by reducing the dark current, and the worst case of radiation-induced degradation is generally expected to happen within a few days after the Total Ionizing Dose (TID) exposure. Those assumptions are based on the most common behavior reported in the literature: a potential small increase in dark current after the end of the irradiation followed by a slow decrease over time that can be accelerated by elevating the temperature (usually at 100°C for 168h). [3] [4] [5]. However, after high temperature annealing, CIS sometimes exhibit a dark current reverse annealing [6], and several papers recently reported, in the case of ultra-high dose on electronics, that annealing, even at room temperatures, could dramatically increase the radiation-induced degradation, eventually making rad-hard electronics inoperable [7]. Annealing inevitably happening with time, the study of these phenomena seems essential, especially for CIS designed to stay in operation for extended periods – such as in space or all the applications cited before.

This paper thus investigates the effect of annealing after applying high doses of radiations (up to 2 MGy(SiO_2)) on different designs of RHBD photodiodes and their embedded electronics. It studies, in particular, the impact of the rad-hard design, the maximum TID, the bias during irradiation, and the annealing temperatures.

II. Experimental Details

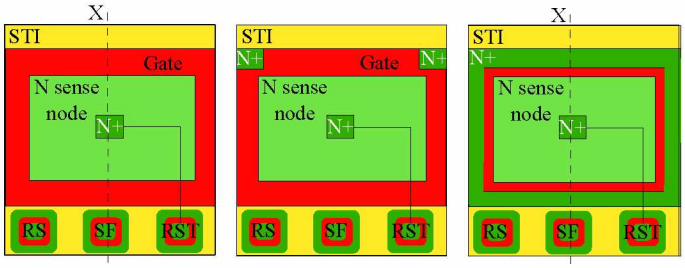
A. Tested CIS

The manufactured 180-nm CIS, developed in 1.8 V technology, are made of 128x256 3T pixels and divided into 16 zones (4 rows and 4 columns) of 32x64 pixels, each of these groups with a different design of photodiode [2].

The first design, presented on Fig. 1a and Fig. 2, is composed, like any classical 3T photodiode (PD), of a photosensitive region, the n-doped sense node, and three transistors designed to reset the signal (RST transistor); amplify it (source follower (SF) transistor); and select the row (row select (RS) transistor) connected to the column readout chain [8]. This PD has been radiation-hardened by design (RHBD) by placing a gate around the photosensitive region (overlapping it), thereby replacing

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(a) Reference PD (b) 2 smalls drains PD (c) PDPD

Fig. 1: Top views of the studied 3-T photodiode designs. The 3 in-pixel transistors (RS, SF and RST) are also represented.

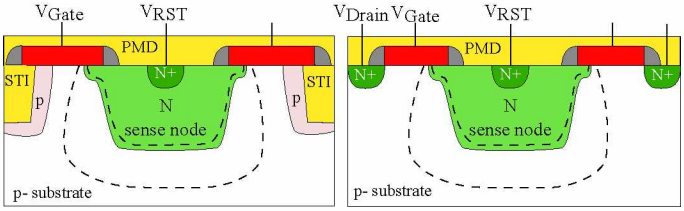


Fig. 2: Cross-sectionnal view of the Ref PD (left) and the PDPD (right) along the axe X.

the Pre-Metal Dielectric (PMD) interfaces with a gate oxide – where a lower density of interface state is expected– and moving away the Shallow Trench Isolation (STI) from the depletion zone. This design has already been proven to be more efficient at mitigating TID effects than existing classical radiation hardened designs [1] [9]. The second design (Fig. 1) add two small n+ drains connected to V_{DD} whereas the third design (Fig. 1c and Fig. 2b) extend these two drains into a peripheral one, completely isolating the depletion zone from the STI. This type of Peripheral Drain PhotoDiode (PDPD) designs has been proven to mitigate some effects of the TID induced dark current [2]. Several intermediate-size drains, from the two smalls drains design to the PDPD, have also been tested and all the designs, except for the PDPD, have been characterized in two versions; with and without inter-photodiode STI. A complete description of these designs is done in [2].

B. Irradiation and Annealing

Six 1.8V CIS have been irradiated, as presented in the table I. Half of them were irradiated "OFF", meaning that no voltage was applied during irradiation, and the other half "ON", meaning that the CIS were acquiring pictures in a standard operation mode. The "OFF" CIS were irradiated with γ-rays while the "ON" CIS were irradiated with X-rays. The expected range of charge yield difference between these two photons energies (possibly down to 25% less degradation with X-rays compared to gamma-rays at the same TID if realistic electric field values are taken into account [10]) is considered insignificant in front of the magnitude of the effects studied here (especially on radiation induced dark current increase where the difference between X and gamma-ray irradiation is usually not visible [9]). The CIS have been characterized before irradiation and in the week following it. Then, an isochronal annealing has been performed, with temperatures varying from 50 to 300°C with steps of 25 or 50°C each lasting precisely 30 minutes. Between each step, the CIS were either tested at room controlled

CIS ID	Voltage	Type	Dose	Dose rate
Cam #1	1.8 V OFF	γ-ray	10 kGy(SiO_2)	0.03 kGy(SiO_2)/h
Cam #2	1.8 V OFF	γ-ray	100 kGy(SiO_2)	0.3 kGy(SiO_2)/h
Cam #3	1.8 V OFF	γ-ray	1 MGy(SiO_2)	3 kGy(SiO_2)/h
Cam #4	1.8 V ON	X-ray	50 kGy(SiO_2)	144 kGy(SiO_2)/h
Cam #5	1.8 V ON	X-ray	300 kGy(SiO_2)	144 kGy(SiO_2)/h
Cam #6	1.8 V ON	X-ray	2 MGy(SiO_2)	144 kGy(SiO_2)/h

TABLE I: Irradiation Conditions

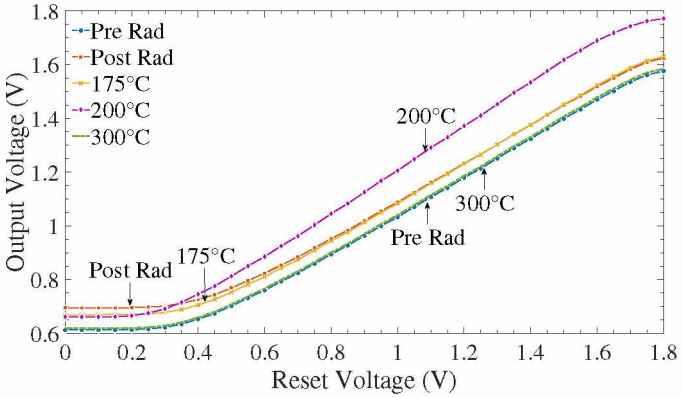


Fig. 3: Evolution of the ETF during annealing after an irradiation at 2 MGy(SiO_2).

temperature (22.5°C) or stored at -18°C to avoid any undesired annealing. The exposed CIS to γ-ray also experienced a 1-year annealing at room temperature before the isochronal annealing. This 1-year annealing leads to approximately the same effect than the 30 min at 50°C step and does not introduce any significant difference in behavior for higher temperature.

III. Radiation Effects on the CIS Electronics

The CIS electronics is the on-chip electronics dedicated to read and amplify the photodiode signal. Its design being the same for all the CIS zones, independently of the pixel design, the results presented in this section are therefore valid for any zone. The CIS electronics have been RHBD by ISAE-SUPAERO using enclosed layout transistors (ELT) for both P- and N-MOSFET, to mitigate the lateral parasitic leakage path and the Radiation-Induced Narrow Channel Effect (RINCE) [11]. The degradation of the readout chain (which represents most of CIS electronics) is studied through the behavior of the quasi-static Electrical Transfert Fonction (ETF) during irradiation and annealing. The ETF is the output voltage of the readout chain as a function of the Reset voltage (V_{RST}) applied on the PD sense node. As discussed in [12], it allows having a first approximation of the readout circuit's degradation. The ETF evolution, after 2 MGy(SiO_2) irradiation and annealing, is presented in Fig. 3, similar trends have been obtained for the other TIDs and irradiation conditions. The ETF degradation can be studied using 3 parameters: the offset (output voltage when the reset voltage is null); the gain (slope of the curve's linear portion); and the swing (linear range of the ETF). The swing, which is directly driven by the two other parameters, is the most important one for the CIS correct operation. Fig. 4 present the evolution of the parameters during irradiation and annealing.

During irradiation, all the parameters are degrading. The offset seems the most sensitive parameter to the dose with degradation of about 13% at 2 MGy(SiO_2) whereas the gain

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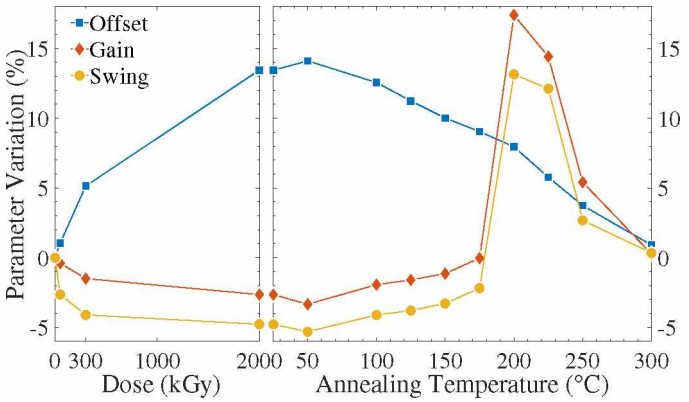


Fig. 4: Evolution of the ETF parameters during irradiation (up to 2 MGy(SiO_2)) and annealing. The evolution during annealing have the same trends for all the CIS.

and the swing have a degradation of respectively about 3% and 5% for the same dose. During the first step of annealing at 50°C, all the parameters degrade slightly more (about 1%). This is observed for all the doses when no 1-year preliminary ambient temperature annealing have been carried out. When it was the case, the degradation is not observed, the reverse annealing being probably already compensated by the positive contribution of the ambient temperature annealing.

After 50°C, all the parameters start improving back to their original value until around 200-225°C where, regardless of the dose, the annealing steps or the 1-year annealing at ambient temperature, the gain suddenly increases leading to a better swing than before irradiation. For the same temperature, the offset sometimes also rebounds but never enough to significantly balance the swing increase. At higher temperatures, the parameters heal again until they almost wholly recover their pre-irradiation value (less than 1% degradation at 300°C). The 200-225°C unexpected behavior has been observed for all the 6 CIS independently of the dose, the photon energy, the bias, the annealing steps or the 1-year annealing at ambient temperature. Non-irradiated CIS have been annealed at the same range of temperatures with no effect, therefore excluding an effect of process-generated defects. To further investigate this phenomenon and since it seems unlikely that the numerical transistor of the readout chain could introduce this effect, a deeper analysis has been performed on the analog transistors of the electronics. The readout chain (for which the complete description is given in [12]) is composed of four models of analog transistors; Two models of bias transistor (N and P) and two models of source follower (both N), each of them present at multiple places in the readout chain. It is possible to measure the bias transistors, and none of them seems to have been particularly affected by the annealing steps around 200°C –i.e., their I-V characteristics is almost the same for the range of temperature 175 to 250°C. The last on the list are thus the source followers; a variation of their transconductance during annealing could explain such an effect, but it is hard to verify their degradation since there is no on-chip access to characterize them directly. This unexpected annealing behavior stresses for a deeper analysis oriented on such rad-hard (ELT) transistors during high-dose irradiation and annealing. In any case, this effect, which actually improves the CIS capabilities, does not

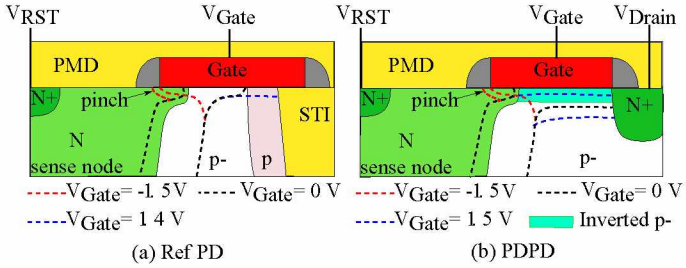


Fig. 5: Cross-section of the Ref PD and the PDPD designs, with the depletion zone for different gate voltages.

compromise its operation and the rest of the measurements as long as they are done in the linear zone.

Overall, in agreement to what could be expected according to the literature [3] [4] [5], the worst-case degradation is observed early during annealing, followed by a slow decrease with time and temperature.

IV. Radiation Effects on the Dark Current

The most limiting effect on the pixels after TID exposure is the increase of the dark current, which is the signal detected by the photodiode in complete darkness. All the measurements in what follows have been performed in a specially dedicated darkroom, at T=22.5°C, and the results presented are the mean dark current over the 32x64 pixels of the specified zone. The dark current I-V curves represent the level of dark current in function of the voltage applied to the gate around the photosensitive region (V_{Gate}).

A. Method of analysis

To ensure a good comprehension of the dark current behavior and a correct interpretation of its evolution during annealing, the following methods have been used to understand and decorrelate the effects of the different parts of the pixel.

1) *V_{RST} variation*: I-V curves are obtained but with lower values of the V_{RST} applied to the PD. By doing so, the reverse bias voltage of the gated-diode-like structure (see Fig. 5a) is lowered. According to the theory [13], a depletion voltage caused by V_{Gate} is expected to be independent of the V_{RST} variation, whereas an inversion voltage should vary proportionally to V_{RST}, which allows to distinguish them.
2) *The null V_{Drain}*: I-V curves are obtained with the drain connected to ground instead of V_{DD}. For the designs without drain, it has no effect, but in the case of the designs with drain (Fig 5b), the structure is now similar to a transistor with V_{RST} as the drain, the V_{Drain} as the source and the gate as the gate. It allows to precisely determine the depletion/inversion of the p- region by V_{Gate} (for all the designs).
3) *Saturation voltage*: The saturation voltage, measured in [2], is the output of the CIS at maximum illumination. It should be constant for all the gate voltage but decreases when the drain leakage is too strong and starts draining the reset signal. This reduction is thus undesired and should always be avoided during operation, but is very convenient to define the V_{Gate} limit for which the drains start to negatively impact the CIS operation.

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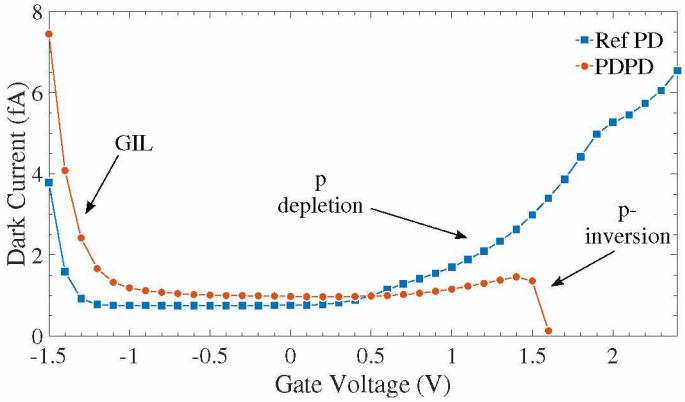


Fig. 6: pre-irradiation dark current as a function of the gate voltage before of the CIS #6. It is similar for all the CIS.

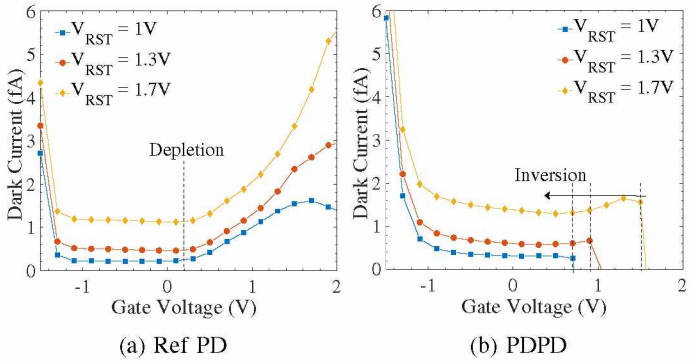


Fig. 7: pre-irradiation dark current as a function of gate voltage for different values of the V_{RST}. The gate induced depletion are constant while gate induced inversion varies with the V_{RST} (The V_{RST} variation method).

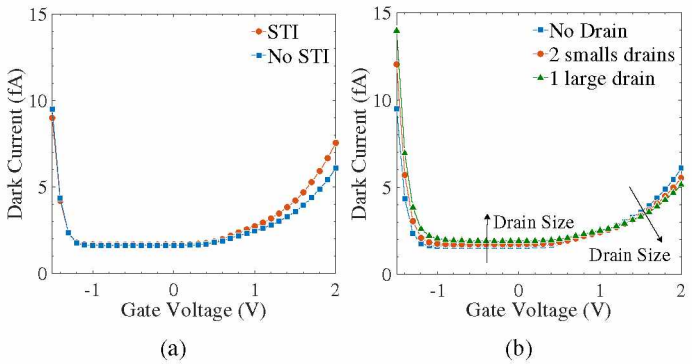


Fig. 8: Effect of the drain (b) and the inter-pixel STI (a) on the pre-irradiation dark current as a function of the gate voltage.

B. Pre-Irradiation

Fig. 6 shows the pre-irradiation dark current as a function of the gate voltage (V_{Gate}) for the reference PD and the PDPD while Fig. 5 shows their cross-section and depletion zones for 3 different V_{Gate} also before irradiation. For intermediate values of V_{Gate} (black line in Fig. 5), the p- region under the gate is depleted, as determined using the null V_{Drain} method. In the case of the Ref PD, the depletion region does not extend up to the STI, due to a p doped region surrounding the STI. This p doped region, already foreseen in [1] [2], is implanted by the manufacturer during the process to passivate the STI sidewalls. Since it is more heavily doped, its depletion voltage V_{dep} is higher, and the complete depletion starts only at 0.2 V. From this point, increasing V_{Gate}, will extend the depletion on the STI interface (blue line going down in Fig. 5a), increasing the dark current proportionally to the STI defect density entering the depletion. If V_{Gate} continues to increase, the p- region under the gate starts to invert. For the reference PD, this means that a part of the gate oxide surface is not in contact with the depleted region anymore (the p region is still not inverted), leading to a negligible reduction of the dark current (the gate oxide being very clean before irradiation) compared to the the continuously increasing dark current due to the contact with the STI. Concerning the PDPD design, there is now a channel open between the PD and the drain (Fig. 5b), which pumps the charge out from the PD. On Fig. 9 the dark current is thus completely suppressed but along with any signal, including the detection current of the photodiode. When V_{Gate} is strongly negative both designs experience a dramatic increase as predicted by the theory [13], due to Gate Induced Leakage (GIL) between the photosensitive region and the gate, provoked by a pinch of the depletion in the photosensitive region (red line in Fig. 5 (a) and (b)). This analysis is comforted as for the same designs but with thicker gate oxide (thus lowering the electric field under the gate for the same voltage) no GIL is observed for the same negative gate voltage.

To support all these assumptions by experiment, the V_{RST} variation method is used. The results, shown in Fig.7, confirm our interpretation. As predicted and experimented by [13], the V_{dep} is independent of the V_{RST} (Fig. 7a) whereas the V_{inv} increases proportionally to V_{RST} (Fig. 7b).

Inter-Pixel STI and Drain Size Effects

Fig. 8a shows the effect of adding inter-photodiode STI on the pre-irradiation dark current. Before depletion, as expected, the additional STI does not influence the dark current, being isolated from the PD by the surrounding p region. Once this region depleted, the dark current increases faster in the design with STI, due to a larger surface between the STI and the depleted region.

Fig. 8b shows the effect of increasing the size of the drain on the dark current. Before inversion, the dark current slightly increases, probably due to a leakage current between the PD and the drain. The larger the drain, the higher the leakage, and the larger the dark current increases. For higher V_{Gate}, since only a part of the STI is isolated by the drain, the design tends to behave like the reference PD design. The larger the drain, the smaller the STI/depletion region surface, leading to a slower increase in the dark current with V_{Gate}.

The different designs provide valuable information to understand more precisely the behavior of the dark current but, since they behave very similarly to the reference PD, they will not be shown in the following figures for the sake of clarity. All the observations for the reference PD are also valid for these designs if not stated otherwise.

C. Post-Irradiation

Fig 9 shows the dark current measurement after irradiation at 50 kGy(SiO_2) for the Ref PD and PDPD. For very negative voltage, no pinch GIL is observable anymore, the positive oxide

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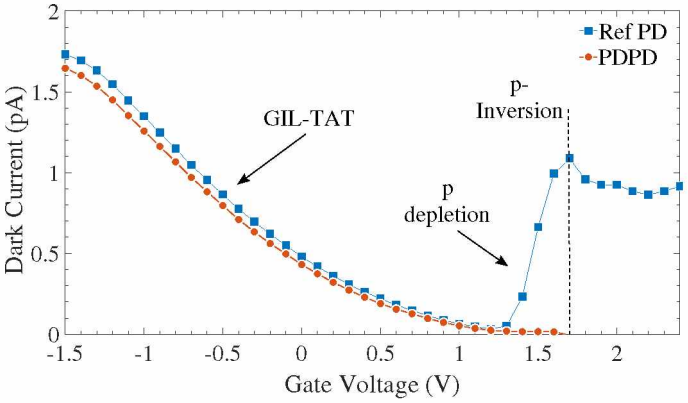


Fig. 9: Dark current of the Ref PD and the PDPD as a function of gate voltage after a 50kGy(SiO_2) irradiation.

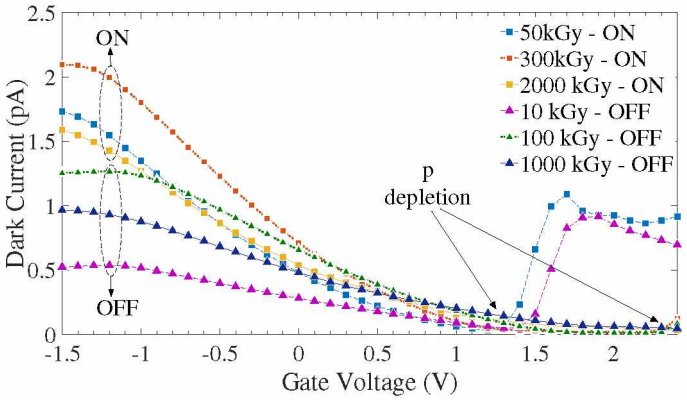


Fig. 10: Evolution of the Ref PD's dark current as a function of the gate voltage for different doses and bias conditions during irradiation.

trap counter balancing the negative V_{Gate} and thus preventing the pinch from happening. However, now a GIL Trap-Assisted-Tunneling (GIL-TAT) appeared over the active photosensitive region of the photodiode. This effect decreases with increasing gate voltage as the potential difference between the gate and the sense node decrease. This GIL-TAT should increase the dark current exponentially, as observed at first, but for strongly negative voltage, the dark current eventually saturates. When V_{Gate} approaches the same value than the V_{RST} of the photodiode (about 1.7 V), and thus suppressing the GIL-TAT, the dark current tends to only be the sum of the generations currents from the the Metal-Induced Junction (MIJ), the Field-Induced Junction (FIJ) and the Surface generation current of the gate [13]. This would be a "theoretical minimum dark current (TMDC)" for the CIS, but is rarely reached in practise, the depletion or inversion often arising for $V_{Gate} < V_{RST}$. Returning to Fig. 9, when the V_{Gate} increases, the ref PD dark current decreases up to the depletion of the p region already observed in pre-irradiation curves but strongly shifted to higher V_{Gate}. This could be due to the increased density of defects in the STI, which influence the electric field of the gate in the ref PD corner area. Indeed, the ref PD gate can be seen as two gates in series: the first one being a simple gate over a p- region, and the second one a gate over the p region with, as oxide, part of the gate oxide and of the STI (due to the overlapping of the gate over the STI and the border field effects). The first gate has a low sensitivity to radiations while the second one is much more sensitive to them due to the STI part. The depletion of the p region, controlled by the "second gate", is thus strongly shifted to higher V_{Gate} even if the gate oxide itself has a low sensitivity to radiations.

Once the depletion reached, the dark current increase with V_{Gate} is steeper also due to the higher density of defects in the STI. When the p- region under the gate is inverting, the ref PD dark current slightly decreases (no gate surface generation dark current over the p- region anymore), but is still dominated by the STI generated dark current. In the case of the PDPD (for which there is no p region nor STI interface), the dark current only decreases up to this inversion where the pumping mechanism already observed pre-irradiation starts, only shifted of around 0.3 V due to the radiation-induced shift of the gate threshold V_{TH}.

Fig. 10 shows the ref PD dark current measurement after irradiation for different doses and bias irradiation condition. Several effects of the dose can be observed. First, the theoretical minimum dark current increases with the dose. This is explained by a higher surface generation current due to a higher density of defects in the gate oxides. Secondly, the GIL-TAT slope first increases with the dose due to higher defects density, but for higher doses (1 and 2 MGy(SiO_2)) the slope is reduced, which could be the result of a higher interface traps concentration. Indeed, independently of the oxide traps (who tends to shift the GIL-TAT regime toward lower V_{Gate}), the interface traps are introducing two phenomena; first they increase the number of centers of generation, thus increasing the dark current. Second, when their concentration increases, their charge starts to be high enough to locally impact the electric field. For low and negative V_{Gate}, the interface traps are charging positively (since located at lower voltage than the midgap), compensating the electric field induced by the negative charges of the gate, therefore reducing the GIL-TAT for a same V_{Gate}. As the number of interface traps has to be high enough to impact the electric field induced by the gate, the second phenomenon is thus observable on the dark current only for higher doses (1-2 MGy(SiO_2)). The last effect of the dose is to shift at a higher V_{Gate} the depletion for the Ref PD due to the creation of defects in the STI (see Fig. 10). It also shifts, to a lesser extend, the inversion voltage for the PDPD due to defects in the gate oxide (not shown here). When the dose is high enough, the irradiation is inducing enough oxide traps in the STI to create an inverted channel around it, acting like a drain, as discussed in [2]. The ref PD and the PDPD dark currents are thus very similar at very high doses (as observed in Fig. 11). The potential gradient induced by the gate is now driving the dark electrons to the drain as it has been numerically simulated in [14] which could explain the observed dark current reduction in Fig. 10 for $V_{Gate} > V_{RST}$ despite the GIL-TAT being already cancelled.

The study of the bias effect is more complex as, in addition to the bias difference (ON/OFF), the CIS were irradiated with different photon energies (X/γ). However, the observed effects seem to be dominated by the difference in bias rather than the photon energy. Indeed, the differences on the observed degradation between the two sets of irradiated CIS are not constant for all the degradation, but they seem to worsen for the ON biased X-ray irradiation where stronger electric fields are present. Since X-ray charge yield is expected to be lower

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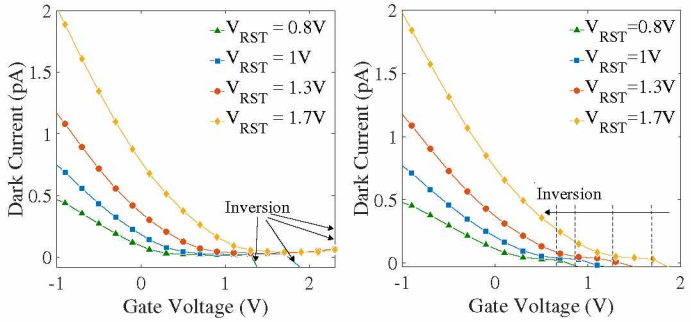


Fig. 11: Post-rad dark current (1 MGy(SiO_2)) as a function of gate voltage for different values of the V_{RST}. The gate induced inversion varies with the V_{RST} (The V_{RST} variation method).

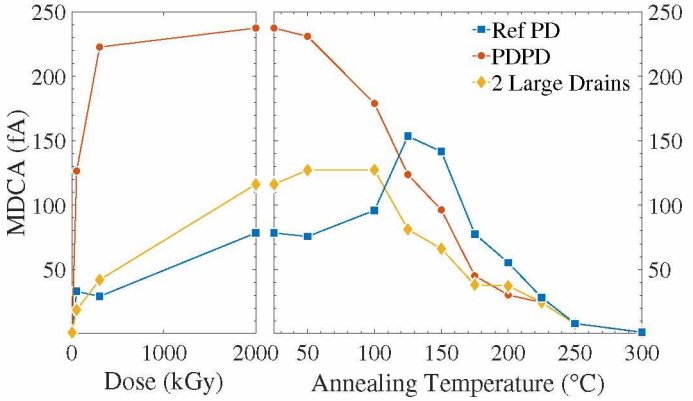


Fig. 12: Evolution of the minimum dark current achievable (MDCA) when tuning the V_{Gate} during irradiation up to 2 MGy(SiO_2) and annealing, for 3 photodiode designs.

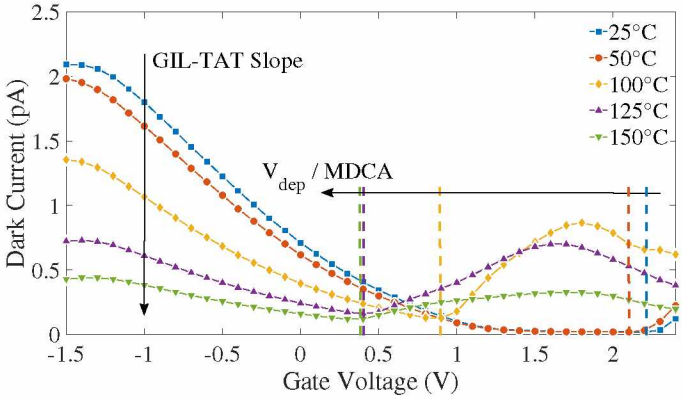


Fig. 13: Evolution of the Ref PD's dark current as a function of the gate voltage during annealing up to 150°C. The CIS was irradiated at 300 kGy(SiO_2).

than the gamma-ray one, this enhanced degradation in the ON biased X-ray irradiation can only be attributed to the additional applied electric field. This leads to believe that the bias effect is dominant over the photon energy difference on the degradation of the CIS dark current. This difference in photon energy will thus be ignored in the following discussion. The first difference between the ON/OFF data-sets is that the GIL-TAT is more severe when the CIS are irradiated in acquisition mode (ON), probably because of the defect generation being higher due a the higher charge yield induced by the potential difference between the sense node region (1.7V) and the Gate Voltage (0V). Second, the shift of the depletion and inversion voltage are the same for both data-sets, in accordance with the gate being grounded during ON and OFF irradiation, therefore not increasing the hole yield with field effect. In third, the TMDC is the same for both bias conditions also due to the absence of field stimulated increased charge yield over the p- and p regions. These assumptions on the post-irradiation curves behaviors of the different designs are again validated by the analysis of the V_{RST} dependency (As shown for example in Fig. 11 for 1 MGy(SiO_2)). The variation of V_{inv} with V_{RST} is observed in both cases, validating that at 1 MGy(SiO_2) both designs are draining the signals (the PDPD through the drain and the reference photodiode through the inversion channel along the STI). Due to the p region, there is a constant difference of around 0.7 V between the inversion voltages of the 2 designs. This high dose radiation-induced drain mechanism seems also confirmed by the apparition of a diminution of the saturation voltage for high V_{Gate} in design without drain when the dose is high enough.

D. Annealing

Fig. 12 shows the evolution of the minimum dark current achievable (MDCA) when properly tuning V_{Gate} during irradiation and annealing. For the Ref PD and all the designs with no or only smalls drains, this minimum is located where the GIL-TAT slope and the depletion meet. During the annealing of the ref PD (blue curve on Fig. 12), the MDCA deteriorates until 125-150°C, where it increases by more than 100% compared to the post-rad value, before healing to almost its original value at 300°C. This behavior is observed at every TID level and for any annealing steps or duration. To understand this behavior, Fig. 13 studies the dark current I-V curves of the ref PD during annealing for a CIS irradiated at 300 kGy(SiO_2). They continuously tend to return to their pre-irradiation behavior, meaning that the theoretical minimum will decrease while the V_{dep} will heal back to its original value (at lower V_{Gate}) and that the GIL-TAT slope will decrease. The part of the curve for $V_{Gate} > V_{dep}$ also anneals; the increase in dark current after the depletion is becoming softer, testifying the annealing of the STI defects and the V_{inv} is healing back to its original value (at lower V_{Gate}).

Fig. 14 studies the evolution of the GIL-TAT slope and the

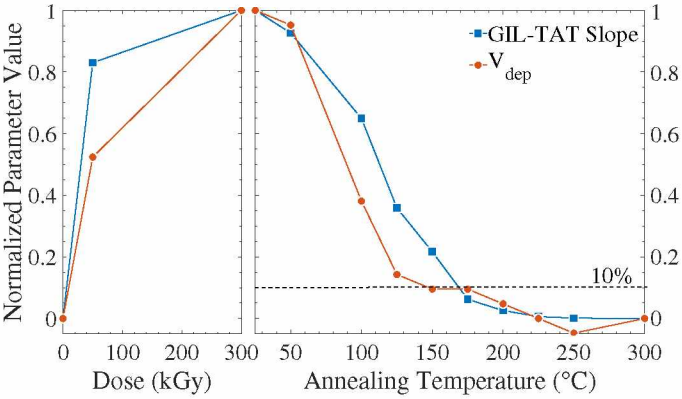


Fig. 14: Evolution of the V_{dep} and the GIL-TAT slope during irradiation up to 300 kGy(SiO_2) and annealing for the Ref PD.

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V_{dep}, the two parameters driving the value of V_{Gate} to achieve the minimum dark current, during irradiation and annealing. These two parameters always heal during annealing, but when the V_{dep} is almost completely annealed for 125-150°C, the GIL-TAT seems to be significantly so only around 175-200°C. It is this difference in the annealing temperature that creates degradation around 125°C observed in the MDCA. Indeed, up to 125°C, as observed on Fig. 13, the V_{dep} healing pushes the MDCA at lower values of V_{Gate}, where the GIL-TAT is stronger and thus increases the MDCA, as the GIL-TAT is healing slower for this range of temperatures. The maximum is reached for 125°C-150°C when the V_{dep} is healed, but the GIL-TAT is still partially unannealed. From there, the depletion voltage is almost not moving anymore, and the MCDA decrease following the annealing of the GIL-TAT. The important point is that even if the parameters are only healing during the annealing, this annealing still degrades the performance of the CIS because of the non uniformity of the parameters annealing temperatures. This behavior is observed independently of the dose, the annealing steps or the 1-year ambient annealing, suggesting that the design architecture is directly driving the annealing behavior. The MDCA for the PDPD and the 2 large drains design is also shown in Fig. 12. For these designs with a drain, the gate voltage applied to reach the MDCA has to be limited by the maximum V_{Gate} before the diminution of the saturation voltage, in order to ensure the correct operation of the CIS. This explain the higher MDCA at post-irradiation, the GIL-TAT being still important for this maximum V_{Gate}. The 2 large drains design seems to be the best in term of MDCA evolution during the irradiation and annealing, mainly due to its higher V_{Gate} limit than the other drain designs, allowing a further reduction of the GIL-TAT compared to these other drain designs. It also reduces the reverse annealing to less than 10%. This behavior is a characteristic of the drain designs and the PDPD even suppresses it (a direct result from suppressing the increase due to the inversion region along the STI interfaces).

Since for some applications a real time tuning of V_{Gate} during operation would be unrealistic, the minimum dark current with a fixed V_{Gate} (MDC_{Vg}) has also been studied. The V_{Gate} has thus been fixed for each zone to the value that minimizes the worst case dark current during irradiation and annealing. The results are presented on Fig. 15. The maximum MDC_{Vg} for the drain designs are the same than when V_{Gate} is tuned, while, for the reference PD, it is worse. Moreover, the 2 large drains design has now always a lower MDC_{Vg} than the reference PD, highlighting the efficiency of the drains designs for real application.

Finally, Fig. 16 shows the dark current curves before irradiation and after the final annealing step at 300°C. It very effectively steers the curve back to its original behavior. Before depletion, the post-annealing dark current is slightly higher in both designs, probably due to some unannealed defects in the gate or spacer oxide. For the reference PD, after depletion, the steeper increase is due to the unannealed defects in the STI. For the PDPD, the inversion happens at the same voltage, testifying the gate V_{TH} recovery with annealing. Similar results have been obtained for all the CIS independently of the dose, the photon energy, the bias during irradiation or the annealing steps and duration. This means that, for any irradiation dose and condition, a 30 min unbiased annealing at 300°C is able to heal very effectively the degradation of the CIS.

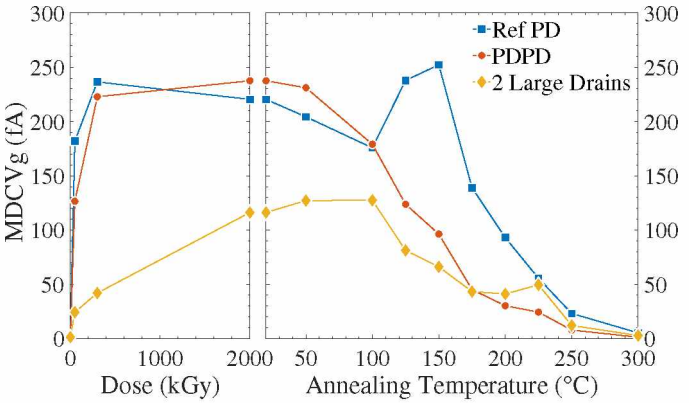


Fig. 15: Evolution of the minimum dark current with a fixed V_{Gate} (MDC_{Vg}) during irradiation up to 2 MGy(SiO_2) and annealing, for 3 photodiode designs.

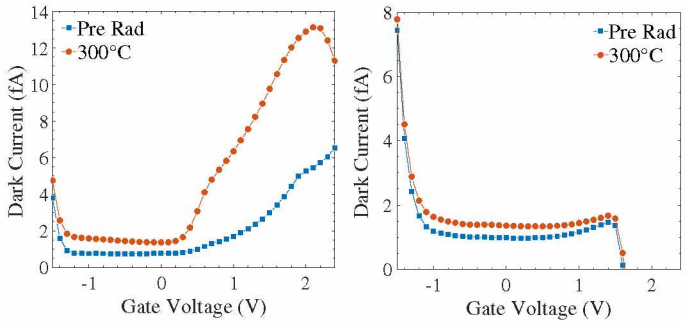


Fig. 16: Dark current as a function of gate voltage, before irradiation at 2 MGy(SiO_2) and after annealing.

V. Discussion

During the annealing of the radiation-hardened CIS, no degradation at the room temperature step has been observed, and the expected latent trapping [5] is either non-existent or too weak to compensate for the ambient positive annealing. However, for higher temperatures, the annealing always degrades the performance of the system. In some cases, such as the 50°C step for the ETF, this is probably due to defects getting worse (latent interface trapping, defect recombination, trapped electron release, dopant passivation [15],...), leading to the typical behavior reported by the literature and observed for the ETF: a small degradation for the first step of annealing, then a constant amelioration. However, as demonstrated in this paper, for complex systems such as CIS, reverse annealing could be the result of a non-uniformity in healing defects, such as, in our case, non-uniformity in annealing temperature. This could lead to more severe degradation than usually expected and could happen at any steps of the annealing, only depending on the design. As we could consider the same phenomena with non uniformity regarding time, or influenced by an electric field, it seems thus highly relevant, when studying irradiation and annealing in complex systems, to be able to isolate the effect of each elementary block, in order to determine, when annealing worsen the degradation, the origin of this degradation – i.e., if it comes from a non uniformity of the different part

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of the system healing or from the apparition of new defects. It also stresses the need to have a good understanding of these elementary elements under radiation and annealing. All of this to adopt the correct hardening solution. As such, this paper demonstrates that designs based only on the analysis of post-irradiation degradation are not able to guarantee CIS operations during their lifetime and that the effect of annealing always needs to be taken into consideration. Moreover, the classic behavior of annealing can not be assumed for complex systems as each difference in design could lead to a very different annealing behavior. The EFT unexpected behavior also illustrates the unpredictable effect of annealing for complex systems and emphasize, once more, the necessity of studying it when designing rad-hard systems. In addition, it has been shown that for all the studied CIS, independently of the annealing degradation, a 300°C unbiased annealing is healing the majority of the defects and is almost fully recovering the minimum pre-irradiation dark current as well as the ETF pre-irradiation behavior.

Isothermal annealing for higher than ambient temperature (e.g. a standard 168h at 100°C [3] [4] [5]) would also be interesting to study. The effects on radiation-induced oxide traps are expected to be the same, only slowed down by the lower temperature [16]. The ones on the radiation-induced interface traps are harder to predict, as being dose and technology dependent [17] [18]. It could still lead to reverse annealing due to non-uniformity but over time instead of temperatures. This reverse annealing could be similar at system levels to the one observed in this paper or different due the different dynamic of the interface traps annealing. Both types of annealing are thus relevant to study when designing complex systems as even if typical field application could be more precisely simulated by an isothermal annealing at the right temperature, isochronal annealing is nevertheless more convenient as it is faster (a 10 min annealing at 225°C correspond to a 16 days annealing at 100°C [16]), allows to cover a larger part of the defects energy spectrum and is more widely used in the literature, therefore more convenient for results comparison [4] [11] [19].

By studying different rad-hard designs, this paper has shown that adding drains to the gated photodiode seems a very promising solution to mitigate radiation and annealing degradation. It allows to diminish the dark current generated by the STI, and even suppress it in the case of the PDPD, both after irradiation and during annealing. In the case of 2 larges drains, it leads to a lower maximum MDCA over all of the irradiation and annealing steps and strongly reduces the dark current increase (from more than 100% to less than 10%) during annealing. The PDPD design even completely suppress this increase. However, the benefits brought by the drain designs are strongly limited by the diminution of the saturation voltage and the draining of the photocurrent. To improve these designs, the V_{dep} and the V_{Gate} limit before loss of saturation voltage need to be pushed at a higher voltage. This could be achieved by increasing the p-doping under the gate, increasing the V_{Gate} limit – ideally as close as V_{RST} as possible – to allow a further reduction of the GIL-TAT. Another way of hardening could be to reduce the radiation-induced increase of the TMDC, by shortening the gate, therefore reducing the gate surface and thus diminishing the surface generation current.

Finally, all the presented observation have been realized on CIS irradiated with the V_{Gate} grounded, but in a real case application, this voltage can be slightly different, as V_{Gate} will be used to minimize the dark current (MDCA or MDC_{Vg}). The effects of biased gate during irradiation need to be studied as it is hard to predict. Indeed, it could increase the charge yield over the p regions, but, at the same time, reduce it over the n regions.

VI. Conclusion

In conclusion, this paper demonstrates that the annealing of complex systems can deteriorate the operation capabilities of these systems, and this at higher temperatures and in a stronger manner than predicted by the literature. The tests presented in this paper have shown that this degradation seems to be caused by a non-uniform behavior of the system parts during annealing, and that therefore this degradation is deeply linked and mainly driven by the system design. With this in mind, this paper also demonstrates the RHBD pixels developed by ISAE-SUPAERO are very efficient to reduce the reverse annealing and are promising for a use in highly radiative environment.

References

[1] V. Goiffon, S. Rizzolo, F. Corbière, S. Rolando, S. Bounasser, M. Sergent, A. Chabane, O. Marcelot, M. Estribeau, P. Magnan, P. Paillet, S. Girard, M. Gaillardin, C. Marcandella, T. Allanche, M. V. Uffelen, L. M. Casellas, R. Scott, and W. D. Cock, "Total Ionizing Dose Effects on a Radiation-Hardened CMOS Image Sensor Demonstrator for ITER Remote Handling," *IEEE Trans. Nucl. Sci*, vol. 65, no. 1, pp. 101–110, Jan. 2018.

[2] S. Rizzolo, V. Goiffon, F. Corbière, R. Molina, A. Chabane, S. Girard, P. Paillet, P. Magnan, A. Boukenter, T. Allanche, C. Muller, C. Monsanglant-Louvet, M. Osmond, H. Desjonquères, J. Macé, P. Burnichon, J. Baudu, and S. Plumeri, "Radiation Hardness Comparison of CMOS Image Sensor Technologies at High Total Ionizing Dose Levels," *IEEE Trans. Nucl. Sci*, vol. 66, no. 1, pp. 111–119, Jan. 2019.

[3] M. Cohen and J. David, "Radiation-induced dark current in CMOS active pixel sensors," *IEEE Trans. Nucl. Sci*, vol. 47, no. 6, pp. 2485–2491, Dec. 2000.

[4] V. Goiffon, C. Virmontois, P. Magnan, S. Girard, and P. Paillet, "Analysis of Total Dose-Induced Dark Current in CMOS Image Sensors From Interface State and Trapped Charge Density Measurements," *IEEE Trans. Nucl. Sci*, vol. 57, no. 6, pp. 3087–3094, Dec. 2010.

[5] S. Dhombres, A. Michez, J. Boch, F. Saigné, S. Beauvivre, D. Kraehenbuehl, J. Vaillé, P. C. Adell, E. Lorfèvre, R. Ecoffet, and F. Roig, "Study of a Thermal Annealing Approach for Very High Total Dose Environments," *IEEE Trans. Nucl. Sci*, vol. 61, no. 6, pp. 2923–2929, Dec. 2014.

[6] M. Beaumel, D. Herve, and D. V. Aken, "Cobalt-60, Proton and Electron Irradiation of a Radiation-Hardened Active Pixel Sensor," *IEEE Trans. Nucl. Sci*, vol. 57, no. 4, pp. 2056–2065, Aug. 2010.

[7] F. Faccio, G. Borghello, E. Lerario, D. M. Fleetwood, R. D. Schrimpf, H. Gong, E. X. Zhang, P. Wang, S. Michelis, S. Gerardin, A. Paccagnella, and S. Bonaldo, "Influence of LDD Spacers and H+Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses," *IEEE Trans. Nucl. Sci*, vol. 65, no. 1, pp. 164–174, Jan. 2018.

[8] E. R. Fossum, "CMOS active pixel image sensors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 395, no. 3, pp. 291–297, Aug. 1997. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900297008127

[9] V. Goiffon, F. Corbière, S. Rolando, M. Estribeau, P. Magnan, B. Avon, J. Baer, M. Gaillardin, R. Molina, P. Paillet, S. Girard, A. Chabane, P. Cervantes, and C. Marcandella, "Multi-MGy Radiation Hard CMOS Image Sensor: Design, Characterization and X/Gamma Rays Total Ionizing Dose Tests," *IEEE Trans. Nucl. Sci*, vol. 62, no. 6, pp. 2956–2964, Dec. 2015.

[10] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for cobalt-60 and 10-keV X-ray irradiations of MOS devices," *IEEE Trans. Nucl. Sci*, vol. 38, no. 6, pp. 1187–1194, Dec. 1991.

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[11] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," *IEEE Trans. Nucl. Sci*, vol. 52, no. 6, pp. 2413–2420, Dec. 2005.

[12] S. Rizzolo, V. Goiffon, M. Sergent, F. Corbière, S. Rolando, A. Chabane, P. Paillet, C. Marcandella, S. Girard, P. Magnan, M. Van Uffelen, L. M. Casellas, R. Scott, and W. De Cock, "Multi-MGy Total Ionizing Dose Induced MOSFET Variability Effects on Radiation Hardened CMOS Image Sensor Performances," in *2017 17th European Conference on Radiation and its Effects on Components and Systems (RADECS)*, Oct. 2017, pp. 1–4, iSSN: 1609-0438.

[13] A. S. Grove, "Surface Effects on p-n Junctions," in *Physics and Technology of Semiconductor Devices*, 1967, pp. 289–316.

[14] O. Marcelot, V. Goiffon, S. Rizzolo, F. Pace, and P. Magnan, "Dark Current Sharing and Cancellation Mechanisms in CMOS Image Sensors Analyzed by TCAD Simulations," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4985–4991, Dec. 2017.

[15] D. M. Fleetwood, M. J. Johnson, T. L. Meisenheimer, P. S. Winokur, W. L. Warren, and S. C. Witczak, "1/f noise, hydrogen transport, and latent interface-trap buildup in irradiated MOS devices," *IEEE Trans. Nucl. Sci*, vol. 44, no. 6, pp. 1810–1817, Dec. 1997, conference Name: IEEE Transactions on Nuclear Science.

[16] C. Chabrerie, J. L. Autran, P. Paillet, O. Flament, J. L. Leray, and J. C. Boudenot, "Isothermal and isochronal annealing methodology to study post-irradiation temperature activated phenomena," *IEEE Trans. Nucl. Sci*, vol. 44, no. 6, pp. 2007–2012, Dec. 1997.

[17] A. J. Lelis, T. R. Oldham, and W. M. DeLancey, "Response of interface traps during high-temperature anneals (MOSFETs)," *IEEE Trans. Nucl. Sci*, vol. 38, no. 6, pp. 1590–1597, Dec. 1991.

[18] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High-temperature silicon-on-insulator electronics for space nuclear power systems: requirements and feasibility," *IEEE Trans. Nucl. Sci*, vol. 35, no. 5, pp. 1099–1112, Oct. 1988.

[19] M. Gaillardin, V. Goiffon, C. Marcandella, S. Girard, M. Martinez, P. Paillet, P. Magnan, and M. Estribeau, "Radiation Effects in CMOS Isolation Oxides: Differences and Similarities With Thermal Oxides," *IEEE Trans. Nucl. Sci*, vol. 60, no. 4, pp. 2623–2629, Aug. 2013.

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