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On Wafer Millimetre Wave Power Detection Using a PN Junction Diode in BiCMOS 55 nm for In-Situ Large Signal Characterization

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***Abstract* —This paper describes millimetre wave (mmW) on-wafer power detection using dedicated high frequency diode junction with a cut-off frequency (fc) of 400 GHz, integrated in SiGe BiCMOS 55 nm technology from STMicroelectronics. This extraction was performed in order to develop fully integrated power detection for transistor or MMIC large signal characterisation on mmW frequency range above 110 GHz. The power detection is performed by biasing the diode in its forward regime. That allows us to obtain an adjustable voltage responsivity (γ) between 426 V/W and 3836 V/W at 320 GHz on the unmatched diode. In this configuration the corresponding dynamic range can be adjusted depending upon the configuration.**

***Keywords* — power detector, millimeter wave, Large signal characterization, BiCMOS 55 nm.**

I. Introduction

Thanks to progress of Silicon Technology cut-off frequencies, complex integrated circuits are increasingly designed in millimetre-wave frequency range, and beyond 110 GHz. Increasing the system frequency allows higher bandwidth and therefore leads to new applications in the scope of high data rates or THz scanning [1]. The design of such complex systems is based on accurate and reliable models of active devices like MOS or bipolar transistors. These models are extracted and validated by high frequency (HF) measurements, including small signal, large signal and noise characterization. However, these models are based on measurements below 110 GHz and are extrapolated beyond due to the lack of industrial measurement tools at those frequencies. For this purpose, high frequency measurements above 110 GHz are of utmost importance for the validation of such models and circuit design in the mmW frequency range. Large signal characterization aims to extract compression point, power added efficiency and power gain under single tone excitation. In mmW frequency range, calorimeter detectors are typically used because no solutions based on diodes are available up to now. However, due to the long-time of acquisition this is not compatible for industrial use, especially for low power detection. Furthermore, these detectors can be used only in steady state. High frequency power detectors have been reported in the literature, using zero bias Schottky diode (SBD) [2], [3], heterostructure low barrier diode (HLBD) [4] and P-N diode [5]. However, part of these solutions has power limitations or are not compatible with silicon technology for Built-in self-test (BIST) application to perform integrated test. Recently, investigations have been done to perform on wafer large signal characterisation, based on load pull methodology setup using in-situ impedance tuner [6] and high frequency power source [7] up to D band frequency range. In addition, to perform on wafer characterisation, integrated power detector is required with high dynamic range and high voltage responsivity to increase measurement accuracy. For this purpose, this paper proposes and describes mmW in-situ power detection solution in BiCMOS 55 nm STMicroelectronics technology.

II. Test Structure and Small Signal Model Extraction

The device used for on wafer mmW power detection is a P-N junction diode available in BiCMOS 55 nm technology from STMicroelectronics. The test structure is composed of a diode mounted in transmission 2-ports configuration connected to dedicated RF pads through access lines on metal level 8 and vias performing connection between Silicon level and the access lines. Figure 1 shows a photography of test structure.

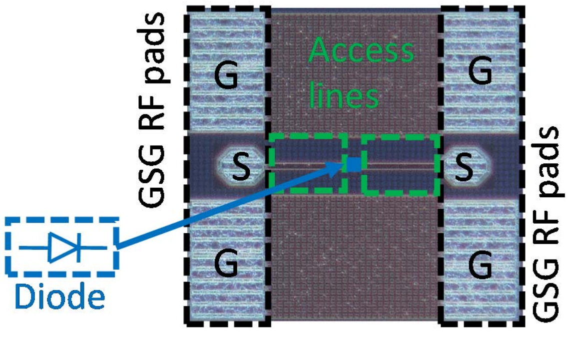

Fig. 1. Test structure photography

Figure 2 shows the test structure model including the intrinsic and extrinsic elements. This model includes: the capacitance of the pads (C_{PAD}), inductance of transmission access lines and vias (L_S), parasitic capacitance between anode and cathode (C_P), resistance and capacitance of the substrate (R_{sub} and C_{sub}), series resistance of the ohmic contacts (R_S) and the resistance and capacitance of the junction (Rj and Cj).

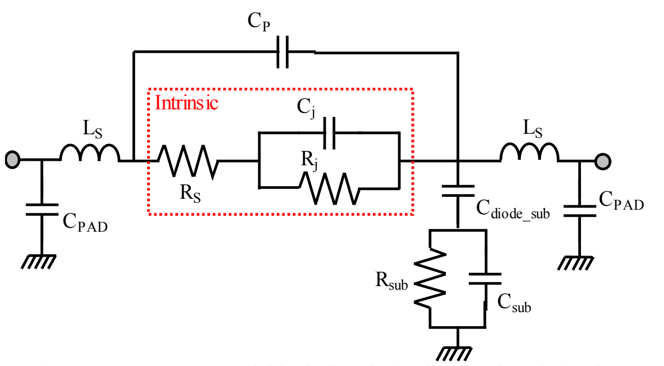

Fig. 2. Test structure model including the intrinsic and extrinsic elements

R_S and R_j can be extracted from the I-V characteristic of the diode, where R_j is deducted from the slope of the I-V curve at a given operating point, and R_s is calculated at relatively high biasing point in the ohmic zone.

A measurement of the S parameters was performed from 0.1 to 110 GHz, in order to extract the values of the model parameters. Extrinsic parasitic elements (C_P, L_S and C_{PAD}) were extracted using open and short dummies. Complete short and complete open are defined on the diode reference planes. L_S is extracted using the complete short structure (RF pads effects de-embedded). Considering the complete open, C_{PAD} and C_P can be extracted. In this study, C_{diode_sub}, R_{sub} and C_{sub} are supposed to be negligible in this frequency range, and the capacitance C_P is supposed to be negligible compared to C_j. All of those assumptions will be validated by comparing the extracted model to the measurements results. Based on the assumptions above, we can consider that the model of the de-embedded diode is the same as the intrinsic model in figure 2. The impedance of the intrinsic model is provided by the equation (1) and C_j can be concluded as the solution of the equation (2).

$$Z = R_s + \frac{R_j}{1+w^2R_j^2C_j^2} - J\frac{wR_j^2C_j}{1+w^2R_j^2C_j^2} \quad (1)$$

$$(imag(Z).w^2.R_j^2).C_j^2 + (w.R_j^2).C_j + imag(Z) = 0 \quad (2)$$

Where w is the angular frequency and *imag(Z)* is the imaginary part of the measured impedance of the de-embedded diode structure. R_j is the junction resistance which is already extracted from the I-V characteristic. Respecting two conditions: (i) that the extraction of C_j is done at high frequency and (ii) having a high value of R_j (which is the case of this study) C_j can be also deducted using equation 3 which gives approximately the same result of equation 2.

$$C_j \approx -\frac{1}{w.imag(Z)} \quad (3)$$

Extracted values of model elements are reported in Table 1 for 1 µA and 5 µA biasing point.

Table 1. Extracted model elements values

Current	**C_{PAD}**	**C_P**	**L_S**	**R_S**	**C_j**	**R_j**
1 µA	3 fF	0.6 fF	30 pH	60 Ω	4 fF	23 kΩ
5µA					6.5 fF	5 kΩ

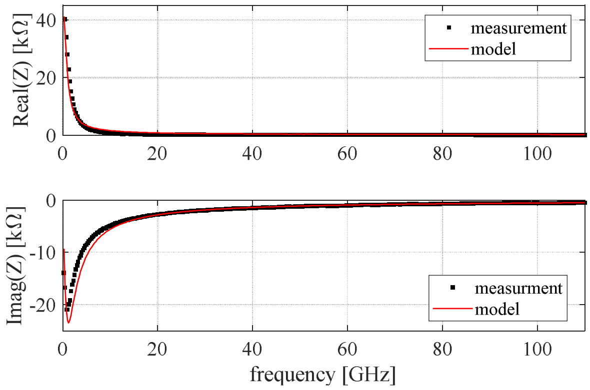

Fig. 3. Real and imaginary part comparison of measured and simulated model of the PN diode junction intrinsic impedance for a biasing voltage of 0.75 V

To validate the model, the element values have been extracted and used to simulate the complex input impedance. These results have been compared to the measurements. Figure 3 shows a comparison between the model and the measured diode impedance. A good agreement is noted over the whole frequency range the fact that confirms our assumptions and validates the proposed model.

III. Large Signal Measurement and Voltage Responsivity Extraction Method

Figure 4 shows the block diagram of the setup used in order to perform on-wafer detection by probing the diode on dedicated RF pads compatible with a pitch of 50 µm. The diode was biased in its forward regime through the integrated bias tee of RF Infinity probes i325. Using a DC source meter KEITHLEY-2440, the bias current was applied and the corresponding DC voltage was measured presenting high impedance (>10 GΩ). The used 300 GHz power source is composed of a frequency multiplier by six and three, which leads to an overall frequency multiplication factor of eighteen, this multiplier is driven by 50-GHz Agilent E8257D PSG, and operating in its compression regime to ensure a constant output impedance. The output power is controlled through mmW manual attenuator.

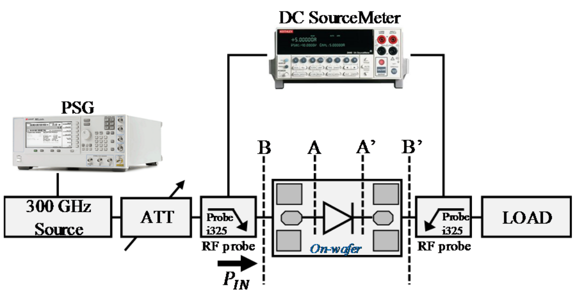

Fig. 4. Test bench block diagram to perform on wafer power detection

Output power calibration was performed after the attenuator, using VDI PM4 power meter; in figure 5 a dynamic power range between -30 and 0 dBm is achieved at 280 GHz. The Input power is defined at RF pads measurement plane, considering RF probe losses and output attenuator power. The 50 Ω mmW load connected after output RF probe helps to minimize any reflection at waveguide interface and stationary waves in the right probe.

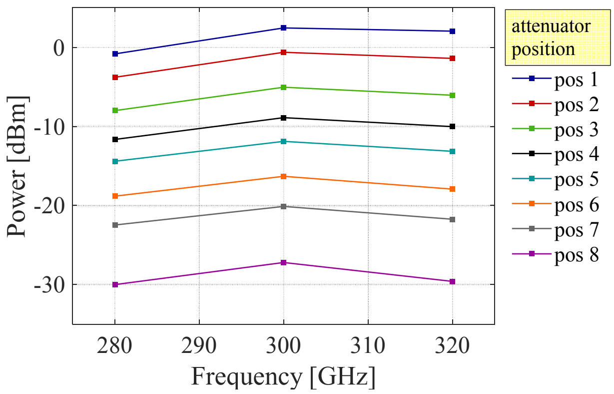

Fig. 5. Available output power of used 300 GHz source

To perform wide frequency range extraction of the on-wafer diode detector sensitivity, the 300 GHz source was substituted by a VNA extender on 220 to 320 GHz frequency range; the latter was used as a power source, providing -30 dBm in the operating frequency range. In case of biased detection operation, the diode is controlled with its DC current. The corresponding voltage value (V_{OFF}) when the power source is OFF, is not equal to zero as shown on figure 6. Hence, when the power source is switched in its ON state, the corresponding voltage value is shifted to (V_{ON}). Thus, the ratio between the delta voltage and the injected high frequency input power corresponds to the sensitivity of the detector (γ), described by equation (4).

$$\gamma = \frac{(V_{OFF} - V_{ON})\,[V]}{P_{IN}\,[W]} \quad (4)$$

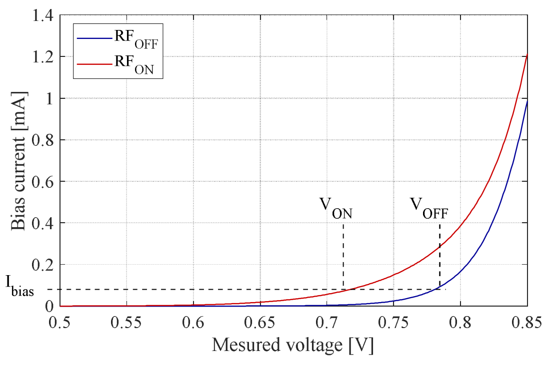

Fig. 6. I-V curves for input constant power at 2 states (RF_{OFF} on blue curve and RF_{ON} on red curve).

Part of measurement uncertainty is related to the DC source meter. The voltage measurement accuracy is defined according to the used voltage range. In our case the 2V range gives a voltage measurement uncertainty $u(V)$ of +/- 300 µV. Second part of extraction accuracy, is related to the assumed input injected power, which is due to source power calibration accuracy. In our case we assume an uncertainty of 5 % of input power related to power calibration and provided by power meter datasheet $u(P_{IN}) = P_{IN}*5\%$. Equation (5) describes the uncertainty $u(\gamma)$ of the corresponding voltage responsivity, by taking into account both $u(V)$ and $u(P_{IN})$. Figure 7 shows the $u(\gamma)$ as a function of the injected power P_{IN}. The uncertainty of the voltage responsivity is dominated by the voltage measurement accuracy of the DC source meter, that take more importance for lower injected powers.

$$|u(\gamma)| = \frac{|u(V)|}{P_{IN} \pm u(P_{IN})} \quad (5)$$

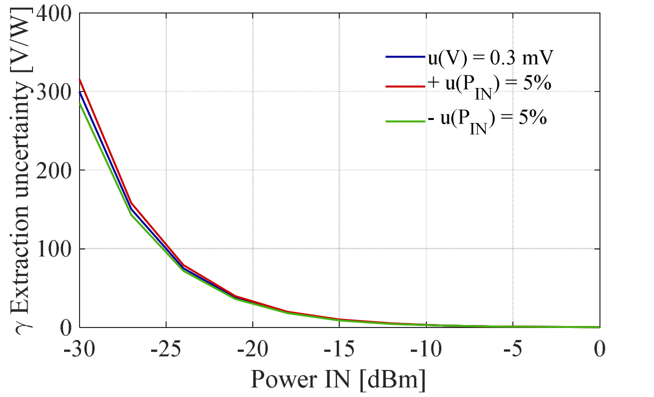

Fig. 7. Measurement uncertainties impact on voltage responsivity extraction function of input power.

IV. Voltage Responsivity Extraction

The voltage responsivity of integrated diode was extracted over 220 to 320 GHz frequency range using VNA extender and mmW power source between 280 GHz and 320 GHz for dynamic extraction. The γ bias dependency measured at 320 GHz plotted in Figure 8 shows a peak of voltage responsivity of 3836 V/W at -33 dBm for a bias current of 1 nA. However, this point is already on saturated regime. Monitoring the bias current condition, the diode features a voltage responsivity varying between 426 to 3836 V/W and allows dynamic range optimisation to increase P_{IN_sat}, corresponding to the power at which the diode saturates. However, the increase of P_{IN_sat} induces a reduction of voltage responsivity.

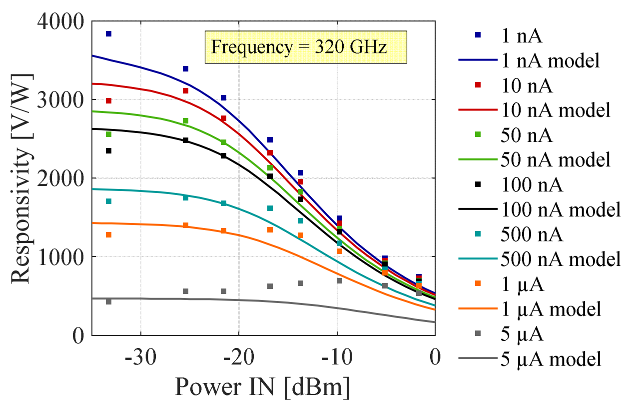

Fig. 8. Extracted and simulated voltage responsivity function of input power for variable bias current at 320 GHz

The previously extracted model was simulated on same configuration by taking into account access line, RF pads and the impedance presented by the probe. The simulated responsivity is close to measured values and has the same bias dependency function of injected power.

Figure 9 shows the extracted and the simulated γ in 220 to 320 GHz frequency range preformed using VNA extender for a bias current of 500 nA. The uncertainty defined previously was accounted for γ extraction. The VNA extender provide around – 30 dBm on pad plane, leading to a $u(\gamma)$ of +/- 300 V/W. We observed discrepancy between extraction performed with 300 GHz source and VNA extender. This is attributed to the presented impedance of the source through the probe on pad plane. To highlight the impedance dependency of this detector configuration, the responsivity was simulated for three configurations; (i) on plane [BB'] taking into account impedance of source through the probe, (ii) on plane [BB'] for a presented impedance of 50 Ohms, (ii) on plane [AA'] for a presented impedance of 50 Ohms. These simulations highlight the dependency of the responsivity on the presented impedance, that inducing ripples on wide frequency range. Table (2) provide performance summary and comparison with prior state of the art.

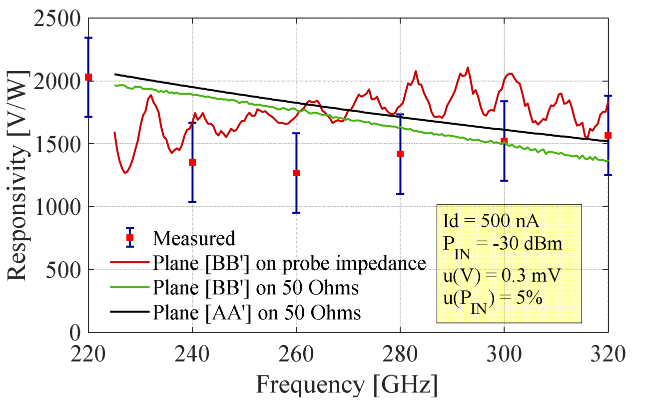

Fig. 9. Simulated and measured voltage responsivity and corresponding uncertainty on 220 to 320 GHz frequency range for a bias current of 500 nA and -30 dBm of input power

Table 2. Detector performances comparison

Technology	Device	NEP (pW/√Hz)	γ (V/W)	Frequency (GHz)	Ref
55 nm BiCMOS	P-N	-	426 3836	320	This work
GaAs	SBD	1.5	4000 400	100 900	[2]
130 nm CMOS	SBD	33	250	280	[3]
AlGaInAs	HLBD	0.7	2000 4000	170 220	[4]
45 nm CMOS	P-N	56	558	781	[5]

V. Conclusion

The described unmatched detector based on diode junction in a BiCMOS 55 nm technology from STMicroelectronics exhibits high voltage responsivity of 3836 V/W at 320 GHz. However, the unmatched configuration leads to high dependence of voltage responsivity on the source impedance. The monitoring of bias current allows wide range γ value and adjustable power detection dynamic range. Study performed on extraction accuracy demonstrates minor impact of measured voltage and power source uncertainties. This study allows potential integration of detector to be used in a wide range of in situ measurement applications such as low noise amplifier, receiver chain, couplers or load pull characterization test structure. The extracted model of the diode was simulated and exhibits a voltage responsivity close to measured values. The model being validated by the aforementioned comparison, it will enable to determine the optimal topologies for the design of more complex detectors.

Acknowledgment

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References

[1] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-Q millimeter-wave passives," in *2014 IEEE International Electron Devices Meeting*, 2014, p. 3.9.1-3.9.3.

[2] J. L. Hesler and T. W. Crowe, "NEP and responsivity of THz zero-bias Schottky diode detectors," in *2007 Joint 32nd International Conference on Infrared and Millimeter Waves and the 15th International Conference on Terahertz Electronics*, 2007, pp. 844–845.

[3] R. Han *et al.*, "A 280-GHz Schottky Diode Detector in 130-nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2602–2612, Nov. 2011.

[4] S. Nadar *et al.*, "High Performance Heterostructure Low Barrier Diodes for Sub-THz Detection," *IEEE Trans. Terahertz Sci. Technol.*, vol. 7, no. 6, pp. 780–788, Nov. 2017.

[5] Z. Ahmad and K. K. O, "THz Detection Using p #x002B;/n-Well Diodes Fabricated in 45-nm CMOS," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 823–826, Jul. 2016.

[6] S. Bouvot *et al.*, "A D-band tuner for in-situ noise and power characterization in BiCMOS 55 nm," in *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2017, pp. 103–106.

[7] A. Bossuet *et al.*, "A 10 dBm Output Power D-Band Power Source With 5 dB Conversion Gain in BiCMOS 55nm," *IEEE Microw. Wirel. Compon. Lett.*, vol. 26, no. 11, pp. 930–932, Nov. 2016.