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Mukherjee Chhandak, Arnaud Poittevin, Ian O'Connor, Guilhem Larrieu, Cristell Maneux. Compact Modeling of 3D Vertical Junctionless Gate-allaround Silicon Nanowire Transistors Towards 3D Logic Design. Solid-State Electronics, 2021, 183, pp.108125. 10.1016/j.sse.2021.108125 . hal-03429568

HAL Id: hal-03429568

<https://hal.science/hal-03429568>

Submitted on 15 Nov 2021

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Compact Modeling of 3D Vertical Junctionless Gate-all-around Silicon Nanowire Transistors Towards 3D Logic Design

Chhandak Mukherjee^a, Arnaud Poittevin^b, Ian O'Connor^b, Guilhem Larrieu^c
and Cristell Maneux^a

^aIMS Laboratory, University of Bordeaux, UMR CNRS 5218, Cours de la Libération - 33405 Talence, France

^bLyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

^cLAAS-CNRS, Université de Toulouse, France

Abstract

To sustain transistor scaling beyond lateral 7nm devices, gate-all-around (GAA) junctionless vertical nanowire field effect transistors (JLNT) are one of the promising alternatives. To overcome the roadblocks of logic cell design using this emerging technology, this work explores compact modeling of 3D GAA-JLNTs based on physics of junctionless transport. The model features an explicit continuous analytical form of drain current calculations adapted for a 14 nm channel junctionless nanowire transistor (JLNT) technology and has been validated against extensive characterization results on a wide range of JLNT geometry, depicting good accuracy. Finally, preliminary simulations have been explored for performance assessment of logic circuits, such as inverters with passive load, active load and complementary topologies as well as ring oscillators, designed using the developed JLNT compact model.

Keywords: Junctionless nanowire transistors, compact model, high-speed logic circuit, heterogeneous integration.

***Corresponding author**

E-mail address: chhandak.mukherjee@ims-bordeaux.fr (Chhandak Mukherjee)

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^bLyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

^cLAAS-CNRS, Université de Toulouse, France

1. Introduction

With increasing demand for data, speed and functionality for computing, hardware performance improvement has become a challenge to cater to the needs of emerging computing paradigms such as neural network, artificial intelligence and edge computing. To sustain scaling beyond the anticipated end of the technological roadmap at the 7nm FinFET node, vertical integration is an attractive approach to overcome the limitations of conventional 2D architectures. Leveraging 3D integration for gate length and contact area scaling [1], junctionless nanowire transistors (JLNT) [2] can circumvent process challenges such as obtaining an abrupt shallow doping gradient at the source/drain junction, ensuring high and uniform body doping and junctionless transition between the channel and the S/D regions. To unlock the full potential of such unconventional 3D technology, logic circuit design relies on accurate physics based compact models that are independent of fitting parameters, that have explicit and continuous solutions over the entire range

of operation and are compatible with existing SPICE design framework. There have been several such modeling approaches for junctionless nanowire transistors, including that of [3, 4], which have mainly focused on long-channel JLNTs. Moreover, most of these works have used TCAD data for model validation, and thus lack validation against experimental data from actual JLNTs. This work presents a compact modeling approach developed based on the physics-based JLNT compact model in [3] adapted for nanowire arrays of short channel JLNTs with gate lengths of 14 nm. The verilog-A SPICE-compatible unified charge-based control model has been self-consistently modified to take into account depletion and accumulation regimes, electrostatic control, access resistances, short-channel effects (SCE), drain-induced barrier lowering (DIBL) and band-to-band tunneling (BTBT) contributions through gate-induced drain leakage (GIDL). Moreover, the model accuracy has been validated against extensive measurements on an emerging vertical JLNT technology from LAAS [1, 5-6] that has

*Corresponding author

E-mail address: chhandak.mukherjee@ims-bordeaux.fr (Chhandak Mukherjee)

been exploited previously for extensive noise characterization [7, 8]. The rest of the paper is organized as follows: Section 2 details the formulation of the compact modeling framework while Section 3 presents model validation, scalability analysis, logic circuit simulation and perspectives for 3D logic cell design, followed by the conclusion.

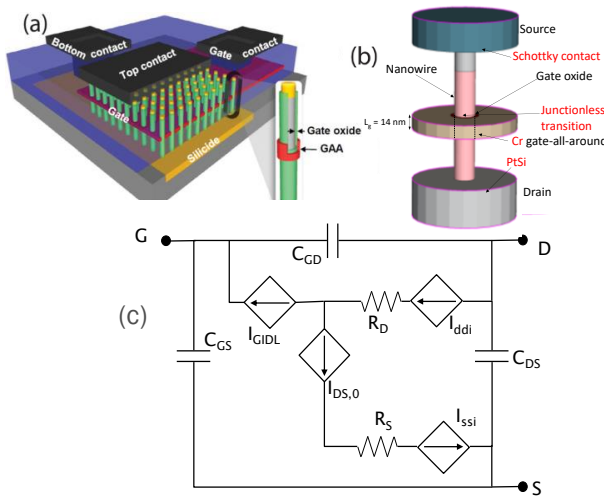


Fig. 1: Schematic representation of (a) vertical junctionless nanowire arrays (reproduced from [7]), (b) geometry of a single nanowire, (c) electrical equivalent circuit of the JLNT.

2. Organization of the Compact Model

The compact model formulation used in this work is based on a unified charge-based control model (UCCM) for long channel junctionless transistors described in [3] adapted for short channel devices. The JLNT technology studied in this work consists of an array of vertical nanowires with top contacts (Fig. 1 (a)) where each nanowire has a gate-all-around architecture with drawn gate length of 14 nm that allows junctionless transition between the channel and the source/drain regions of the nanowire (Fig. 1(b)). The electrical equivalent circuit representation of a

single nanowire is shown in Fig. 1(c) that shows the long-channel drain current, $I_{DS,0}$, connected in series with the drain/source Schottky diode currents, I_{ddi} and I_{ssi} for modeling the Schottky contacts. Additionally, the source/drain access region resistances, R_S , R_D , as well as the gate-induced drain leakage current, I_{GIDL} , contributions are taken into account for the model formulation. Firstly, the UCCM formulation of [3] describes long-channel single nanowire devices, which furthers the physical basis of the JLNT model presented in [4]. To overcome the limitations of the latter model, specifically in terms of the piece-wise continuous drain current model that requires additional smoothing functions and fitting parameters to bridge the depletion and accumulation modes of operation, the explicit and non-piece-wise solution in [3] treats the mobile charge (Q_m) as decoupled between the depletion (Q_{DP}) and complementary (Q_C) components. In the depletion mode the UCCM expression has been formulated as [3],

$$Q_{DP} = Q_{eff} LW \left\{ \frac{Q_{sc}}{Q_{eff}} \exp \left(\frac{V_g - V_{th} - \eta V}{\eta \phi_T} + \frac{Q_{dep}}{Q_{sc}} \right) \right\} \quad (1)$$

With the depletion charge, $Q_{dep} = qN_D R/2$, the effective charge during depletion, $Q_{eff} = Q_{sc} \eta C_{ox} \phi_T / (Q_{sc} + \eta C_{ox} \phi_T)$, $Q_{sc} = 2\epsilon_{Si} \phi_T / R$, R being the nanowire radius, η being an interface trap parameter, ϕ_T being the thermal voltage and V is the potential along the channel. Lambert W functions, LW, have been used in both [3] and [4] for developing the solution for the total mobile charge in the JLNT. While the expression for Q_{DP} in (1) predicts the depletion contribution correctly (for $V_g < V_{th}$), it underestimates the value of the drain current above the flat-band condition. So in accumulation mode,

especially in high accumulation, with $Q_C \geq Q_{dep}$, the charge Q_C has been derived to act complementary to Q_{DP} , considering that the threshold voltage is pinned at V_{FB} in the accumulation region, in order to avoid using additional smoothing functions and improve simulation time. Under high accumulation $Q_C \geq Q_{dep}$ and Q_C is simplified using another Lambert function as following [3],

$$Q_C = \eta C_c \phi_T LW \left\{ \frac{Q_{sc}}{\eta C_c \phi_T} \exp \left(\frac{V_g - V_{FB} - \eta V}{\eta \phi_T} \right) \right\} \quad (2)$$

With corrected electrostatic control through $C_c = C_{ox} - C_{eff}$, $C_{eff} = 1/C_{ox} + R/2\epsilon_{Si}$.

Having evaluated both the depletion and complementary parts of the mobile charge, one can formulate the non-piece-wise continuous model of the total drain current in terms of the Q_{DP} and Q_{DC} at the source and the drain end, Q_{DP0} , Q_{C0} and Q_{DPL} , Q_{CL} , respectively,

$$I_{DS,0} = \mu_{eff} \frac{2\pi R}{L_{eff}} \left[\int_{Q_{DP0}}^{Q_{DPL}} Q_{DP} \frac{dV}{dQ_{DP}} dQ_{DP} + \int_{Q_{C0}}^{Q_{CL}} Q_C \frac{dV}{dQ_C} dQ_C \right] \quad (3a)$$

From the derivatives of the logarithm of both sides of eqs. (1) and (2) one can write,

$$\frac{dV}{dQ_{DP}} = -\phi_T \left[\frac{1}{\eta C_{ox} \phi_T} + \frac{1}{Q_{DP}} \right], \frac{dV}{dQ_C} = -\phi_T \left[\frac{1}{\eta C_c \phi_T} + \frac{2}{Q_C} \right] \quad (3b)$$

Finally, combining (3a) and (3b), the equation of the drain current reads,

$$I_{DS,0} = \mu_{eff} \frac{2\pi R}{L_{eff}} \phi_T \left[\frac{Q_{DP}^2}{2\eta C_{ox} \phi_T} + Q_{DP} + \frac{Q_C^2}{2\eta C_c \phi_T} + 2Q_C \right]_{Q_{DP0}}^{Q_{DPL}} \quad (3c)$$

Here, η is an interface trap parameter with corrected electrostatic control in accumulation through $C_c = C_{ox} - C_{eff}$, $C_{eff} = 1/C_{ox} + R/2\epsilon_{Si}$. Additionally, short channel effects were also taken into account considering

velocity saturation, an effective mobility, μ_{eff} , and incorporating an effective gate length, $L_{eff} = L - \Delta L$, where L is the physical device gate length and ΔL is calculated following [9],

$$\Delta L = S \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}} \ln \left[\frac{(V_d - V_{def}) \left(1 + \sqrt{1 + \left(\frac{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}}}{V_d - V_{def}} \right)^2} \right)}{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}}} \right] \quad (4)$$

Note that for parameter initialization, carrier mobility values for nanowire transistors were adopted from [10]. However, due to the increased scattering in highly doped nanowires owing to a junctionless architecture and possible mobility collapse in small gate lengths [7, 11], carrier mobility values are found to be significantly lower than expected. The final values used in the model parameter set were obtained from fitting against measurement results. Here, v_{sat} is the saturation velocity and S is a parameter ensuring that ΔL tends to zero below the threshold, defined as [9],

$$S = \sqrt{1 - \frac{1}{1 + B \frac{Q_{DP0} + Q_{C0}}{C_{eff} \phi_T}}} \quad (5)$$

Where $Q_{DP0} + Q_{C0}$ is the total mobile charge at the source, given by the long channel expression and B is a smoothing parameter. Furthermore, the short channel corrections incorporates an effective drain voltage, V_{def} , through (4) that reaches its maximum at V_{SAT} , the saturation voltage [9],

$$V_{def} = V_{SAT} - V_{SAT} \frac{\ln \left(1 + \exp \left(A2 \left(1 - \frac{V_d}{V_{SAT}} \right) \right) \right)}{\ln(1 + \exp(A2))} \quad (6)$$

Here, A_2 is another smoothing parameter for the transition of the drain voltage to V_{SAT} . Considering that the source and drain access region resistances degrade the drain current above threshold, the final expression of the drain current can be written as a function of the long channel current ($I_{DS,0}$), using (3c), taking into account the corrections due to short-channel effects described by equations (4)-(6), as follows [9],

$$I_{DS} = \frac{I_{DS,0} NF}{1 + 2\pi \frac{R}{L_{eff}} NF \mu_{eff} (R_S + R_D) [(Q_{DP0} + Q_{C0}) - \eta_1 (Q_{DP, V_{deff}} + Q_{C, V_{deff}})]} \quad (7)$$

Here, R_S and R_D are the source and drain series access resistances, respectively; NF is the number of nanowires in parallel, η_1 is a fine-tuning parameter to take into account the drain-voltage dependence of the series access resistances and $Q_{DP, V_{deff}} + Q_{C, V_{deff}}$ is the total mobile charge at the drain end (pinch-off) of the channel. In [3], the expression of long-channel drain current is developed free of any fitting parameters. However, to adapt equation (3c) in the context of a short channel device, both L_{eff} and μ_{eff} are further recalculated involving the two smoothing parameters, A_2 and B , which are quite common in the context of ensuring compact model stability and convergence. The UCCM formulation is particularly suitable for the aforementioned reasons of a compact modeling viewpoint and can be evaluated based on the physical device parameters such as geometry and doping.

Additionally, considering formation of Schottky contacts at the source and drain access regions, the subthreshold leakage currents are also taken into account. Therefore, thermionic (I_{th}), tunneling (I_{tun}) and band-to-band tunneling (BTBT) contributions through gate-induced drain leakage

(GIDL) are added as separate branch currents [12] to the total drain current (Fig. 1(c)), in order to model the subthreshold behavior of the drain current. The expression used in the compact model for the BTBT current at the drain end reads [12],

$$I_{GIDL} = 2\pi R L_{Access} NF \cdot A_{GIDL} V_{DS} E_{segd}^2 \exp\left(-\frac{B_{GIDL}}{E_{segd}}\right) \quad (8)$$

With L_{Access} being the lengths of the source and drain access regions outside the channel, B_{GIDL} is a physics based parameter with a theoretical value of 21.3 MV/cm [12] and E_{segd} is the electric field in the drain overlap region, given as,

$$E_{segd} = \frac{C_{ox} \sqrt{V_{segd}^2 + (C_{GIDL} V_{DS})^2}}{\epsilon_0 \epsilon_{Si}} \quad (9)$$

Here, V_{segd} is the gate-drain voltages across the oxide and A_{GIDL} , C_{GIDL} are two GIDL fitting parameters.

Finally, additional model improvement has been achieved compared to the preliminary version of the model [13], especially in the subthreshold regime. In order to improve model accuracy, the accurate extraction of the parameter η is ensured in order to correctly adjust the subthreshold slope. Moreover, the effect of drain-induced barrier lowering (DIBL) is also taken into account in the compact model by a modification of the threshold voltage through the following equation,

$$V_{th} = V_{FB} - \frac{Q_{dep}}{C_{ox}} - DIBL(V_{DSmax} - V_{DSmin}) \quad (10)$$

with $DIBL$ being the drain-induced barrier lowering.

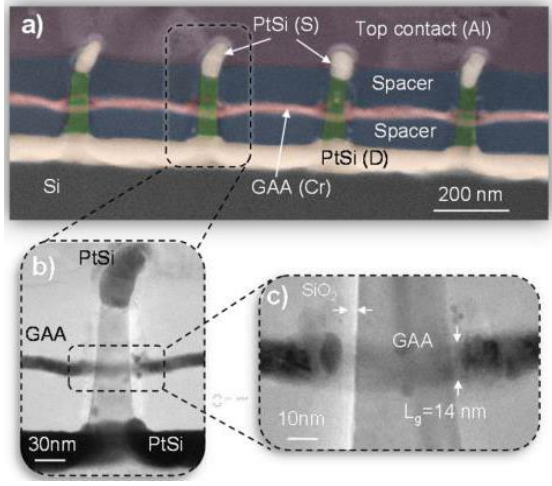


Fig. 2: The vertical JLNT: (a) SEM image of nanowire arrays, (b) single nanowire showing (c) gate formation (reproduced from [1]).

3. Results and Discussions

From the compact model formulation point of view, this work is mainly focused on establishing consistency between the adopted modules of the modeling framework. From the point of view of developing a process design kit (PDK), the focus remains on parameter extraction and model validation on an actual junctionless transistor technology which, unlike previous attempts of model development in comparison with TCAD simulations, offers a stronger validation of the compact model. Overall, the main focus is not just a compact model for junctionless transistors, but to offer a larger perspective on design approaches for 3D non-conventional logic circuits using a vertical junctionless nanowire technology, which is also inherently 3D in nature, for future computing paradigms. The present work is just the first step for clearly defining the value chain of such design flow. Note that, the parameter extraction process used in this work could also be used for other

similar technologies, which is very useful for the design community.

3.1. The JLNT Technology

The junction-less gate-all-around nanowire transistor technology [1, 5] is composed of a homogenous highly doped nanowire channel, patterned into boron doped ($2 \times 10^{19} \text{cm}^{-3}$) Si-substrate. Current between silicided source/drain contacts is controlled by a gate-all-around structure with physical channel length of 14 nm (Fig. 2). As illustrated in the 3D schematic of a 1-bit adder logic cell consisting of vertically stacked JLNTs, vertical integration allows higher flexibility over lateral devices in terms of gate, spacer and channel lengths without compromising on cell area, thus paving the way for scalable and innovative logic designs. Process parameters for the JLNT under study are summarized in table I.

TABLE I: PROCESS PARAMETERS FOR THE JLNT UNDER STUDY

Process Parameter	Value
Physical gate length	14 nm
NW diameter	22 nm
NW in parallel	16
T_{ox}	5 nm
N_{ch}	$1.1 \times 10^{19} \text{cm}^{-3}$
Gate work function	4.5 eV

3.2. Compact Model Validation

The compact model formulation presented in the previous section is validated against measurement results on a wide range of geometries and test structures that have diameters (D) ranging between 22 and 50 nm with 16 to 625 nanowires in parallel (NF). Here we show model validation results from nanowires of 22 nm diameter with different number of

nanowires in parallel. Figs. 3 (a) and (b) show the I_D - V_{GS} and I_D - V_{DS} of a JLNT with 22 nm of nanowire diameter and 16 nanowires in parallel. The model simulation results show very good agreement with the measurements over the entire bias range, indicating accuracy of individual modules of the compact model. A second order validation is performed in Figs. 3 (c) and (d) depicting the transconductance, g_M , and output conductance, g_{DS} , of the JLNT, further affirming model accuracy, despite a somewhat noisy measurement.

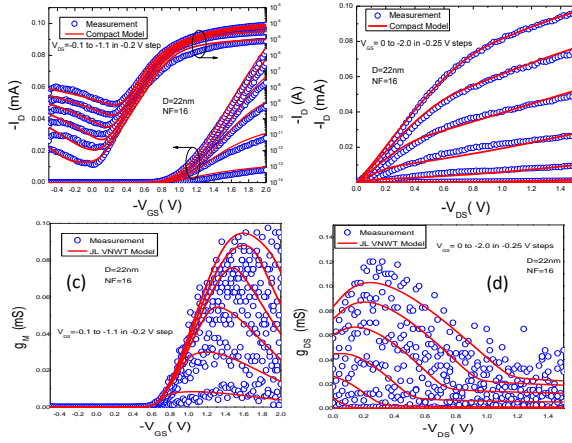


Fig. 3: (a) I_D - V_{GS} , (b) I_D - V_{DS} (c) transconductance and (d) output conductance of a JLNT of $D = 22$ nm and 16 nanowires in parallel.

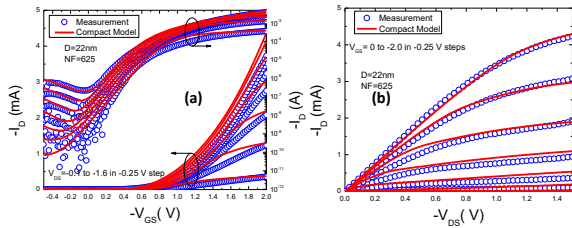


Fig. 4: (a) I_D - V_{GS} , (b) I_D - V_{DS} of a JLNT with test structures having a diameter 22 nm and 625 nanowires in parallel.

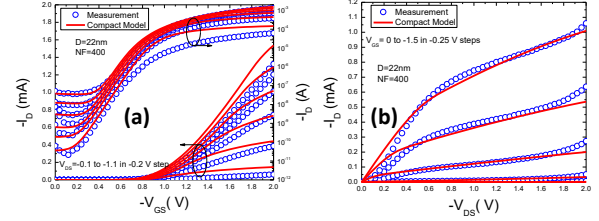


Fig. 5: (a) I_D - V_{GS} , (b) I_D - V_{DS} of a JLNT with test structures having a diameter 22 nm and 400 nanowires in parallel.

Extended model validation has been performed on two other test structures, with different geometries available from the same technology. Figs. 4 (a) and (b) show the I_D - V_{GS} and I_D - V_{DS} of JLNT test structures with a diameter of 22 nm with 625 nanowires in parallel. Good model agreement is obtained in this case as well. Similar validation is depicted in Fig. 5 for a JLNT test structure with a diameter of 22nm and 400 nanowires in parallel, again depicting good agreement with the model simulation.

Note that, in the subthreshold and linear regions, the uncertainty in model simulation is indeed higher compared to the saturation (high V_G , V_D) region and therefore slight variation in parameters, such as access resistances or leakage current parameters, result in an observable deviation between the model and the measurements. The results shown in this work are obtained for the best-case optimization scenarios that describe the overall curves with sufficient accuracy. Globally for all the simulated voltage and currents, the error does not exceed 10%, which is denoted as a good agreement, and which is also the maximum permissible error in the context of industrial electronics, even though ours is an academic technology.

3.3. Towards Current Scalability

Model scalability is crucial for compact models to support predictive design at circuit level. It further allows the extraction of a scalable model parameter set that can be used for innovative logic circuit design. Even though the present model formulation is inherently scalable, given the maturity of the technology, the measured drain current does not scale across all devices under test. As depicted in Fig. 6 (a), the normalized (with the effective NW width, $\pi D \times NF$) drain current shows scalability for mainly devices with diameters of 22 nm (the representative set from this technology). The deviation from linearity in larger diameters could possibly be attributed to process variation.

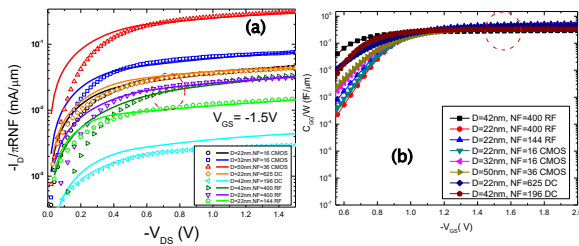


Fig. 6: (a) Drain current and (b) total gate capacitance of JLNT normalized with NW effective width.

Another observation is that the current scales better in terms of number of nanowires in parallel and with a reduction of the NW diameter (lower DIBL, improved SS slope), better JLNT scaling can be observed. On the other hand, the total gate capacitance extracted from the compact model fit, shows better scalability over all geometries under test (Fig. 6(b)). This indicates that the intrinsic charges scale better than the total drain current, the latter of which does not scale well owing to the presence of additional effects (such as access contributions, leakage currents etc.). To

achieve better current scalability, certain aspects of the process could be further improved to ensure better process uniformity in the subsequent runs of this academic technology. Overall, in future iterations of this modeling framework, the focus will remain on deriving and clearly identifying the scaling laws in a 3D vertical structure (by nature) such as this technology in comparison with conventional MOSFETs for which the scaling laws are mainly 2D. The future versions of this model will thus take in to account the 3D integration mode as well as parasitic elements within the 3D structure.

3.4. Logic Performance Assessment

In this section, we leverage the developed compact model for assessing the performances of various topologies of an elementary inverter constructed using the JLNT technology. To fully assess the design specific issues that could be present in such an emerging technology, we limit the logic circuit analysis to such elementary architecture. The main goal of this study is to evaluate the performance of the model in scenarios of classical logic circuit architectures and study their key performance metrics. To be able to do it, one of the important aspects was to evaluate the compatibility of the verilogA model with classical circuit simulators such as CADENCE. During this step, simulation convergence issues have also been assessed that allowed us to determine the model's computational efficiency. Even though, these classical logic circuit simulations are simply a standard method of validation of the modeling framework, as mentioned before, the ultimate goal is non-conventional 3D logic design and to demonstrate area/power optimized

computational logic cells for future computing. This part thus remains a mandatory step for future advancements. Moreover, due to lack of complementary transistor data, more complex architectures are not explored and we focus on the simulated performance of p-type only inverters. In the following study, a simple complementary inverter is investigated through model extrapolation to n-type transistor following CMOS design conventions.

For both the p-type only inverter structures investigated, a p-type JLNT has been used as a conventional pull-up, while the pull-down branch has been implemented either by an active p-type device load or a resistive, i.e. a passive load. In the first case, the p-type device load has been configured as a current source. Fig. 7(a) illustrates the 3D layout of the vertical inverter structure with active load, offering perspectives into how area optimization and compactness in 3D logic circuits can be addressed using the vertical JLNT technology [14]. In order to optimize interconnect lengths, the bottom layer of the structure connects the drains of the pull-up and load transistors where the output voltage can be measured, while the two sources are contacted at the top layer (Fig. 2). The gate contacts are taken at the middle layer to supply the input (V_{IN}) and control voltages (V_{GLoad}).

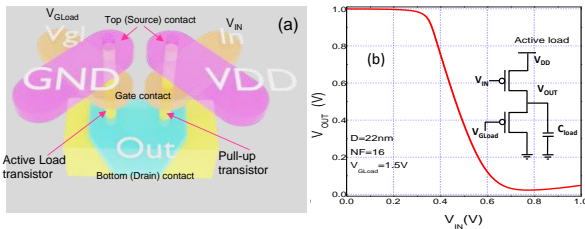


Fig. 7: (a) Schematic 3D view of the layout and (b) voltage transfer characteristics of a p-type only inverter with active p-type JLNT load.

The inset of Fig. 7(b) illustrates the schematic circuit representation of the inverter in Fig. 7(a) using active p-type device biased as a current source with an input (gate) control voltage as well as the pull-up transistor. Both transistors have dimensions of $D=22nm$ and $NF=16$ and the active load has been biased with a positive gate voltage, V_{GLoad} , of 1.5V. The voltage transfer characteristics (VTC) of the inverter has been shown in Fig. 7(b) that shows a symmetrical logic level transition at around 0.5V of V_{IN} . However, a logic 0 degradation can be observed from the VTC. It has also been observed that increasing the V_{GLoad} improves the logic 0 degradation; here the value 1.5V has been chosen as optimum since beyond this value no further improvement is significant. The degradation is likely due to the series resistive contribution at the bottom layer where the outputs are measured (Fig. 7(a)).

Fig. 8 (a) shows the VTC of the passive load inverter (the schematic is shown in the inset), designed using p-type devices with nanowire diameter of 22nm and 16 nanowires in parallel and a resistive load of 200 M Ω . Similar to Fig. 7(b), the results show a symmetric switching characteristic (at $V_{IN}=0.5$ V) with slightly degraded low logic state. For both resistive and active load inverters, the pull-down load is responsible for the low logic state output. While these architectures are known to be less efficient compared to their complementary counterparts, they are suitable for design validation of logic circuit using experimental data. For the complementary inverter, we extrapolated the model simulation for n-type JLNT considering a carrier mobility 3 times that of the p-type JLNTs [2, 13]. Hence to balance the circuit for a switching input voltage value halfway between the supply rails and for

roughly equivalent noise margins and identical currents in both devices, we chose NF (number of nanowires) per device in the p-type equal to 2x that of the n-type.

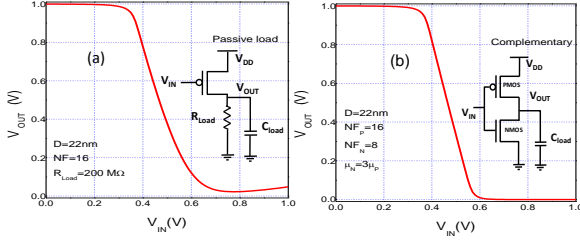


Fig. 8: Voltage transfer characteristics of (a) p-type only resistive load and (b) complementary inverter.

The conventional CMOS inverter configuration, using a n-type device load, has been studied in Fig. 8 (b). The results indicate again an almost symmetric logic high to low transition. Slight asymmetry in the complementary configurations indicates that simple extrapolation to n-type devices following CMOS design conventions is not as efficient, as different model parameters were not optimized for the n-FETs. Model parameters can be further refined using experimental data of n-type devices from subsequent technology generations, for better prediction of complementary circuit performances. Nonetheless, using a complementary inverter configuration improves the logic-0 degradation compared to the passive and p-type active load configurations. As shown in Fig. 9 (a) the low-level logic degradation (5-10%) is evident in case of p-type only configurations due to the design limitation of the pull-down elements. The pull-down n-type device in the complementary CMOS configuration ensures very little logic 0 degradation. Fig. 9 (b) compares the transient response of the CMOS inverters designed using the

extrapolated model. The model prediction for a complementary CMOS inverter closely matches with the results reported in our previous works [5, 6] that demonstrate a proof-of concept CMOS inverter consisting of both n- and p-type JLNTs.

Next, we extracted the performance metrics such as static leakage current density and I_{ON}/I_{OFF} ratios of the JLNT technology. The static leakage current density is a crucial parameter for minimizing off state power dissipation and thus the overall dynamic power consumption. Static leakage current density of the order of 0.16-0.174 $\mu A/\mu m^2$ has been extracted from model simulation. On the other hand, the I_{ON}/I_{OFF} ratios were extracted in the range of $0.65\text{-}0.66 \times 10^4$. These values are summarized in Table II, in addition to the metrics related to computational complexity.

Table II. Inverter Cell: Performance and Computational Metrics

Metric	Value
Static leakage current density ($\mu A/\mu m^2$)	0.174
I_{on}/I_{off} ratio ($\times 10^4$)	0.66
CPU time for elementary logic cell (s)	0.12
Total number of model parameters	23

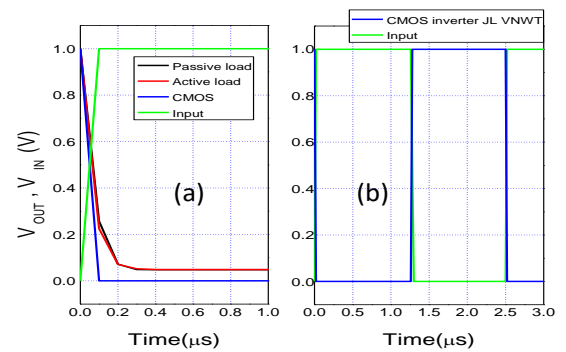


Fig. 9: Transient simulation comparing the outputs of (a) p-type only and complementary CMOS inverters and (b) input and output waveforms of the CMOS inverter.

Finally, we have studied a 9-stage ring oscillator consisting of 9 inverter stages in cascade. Each inverter of the ring-oscillator has the same

characteristics as shown in Fig. 7 (b). In Fig. 10, the outputs of the different stages of the ring oscillator are shown on the voltage transfer characteristics (VTC). As observed from the figure, the output of the first stage resembles the VTC of the single stage inverter (Fig. 7 (b)), while the high-to-low transition continues to be sharper from one stage to the next. Although, the output of the 9th stage shows almost no switching dissipation, from the output of the third stage onwards the transitions are quite similar and sharp. This indicates that the optimum number of stages required is 3.

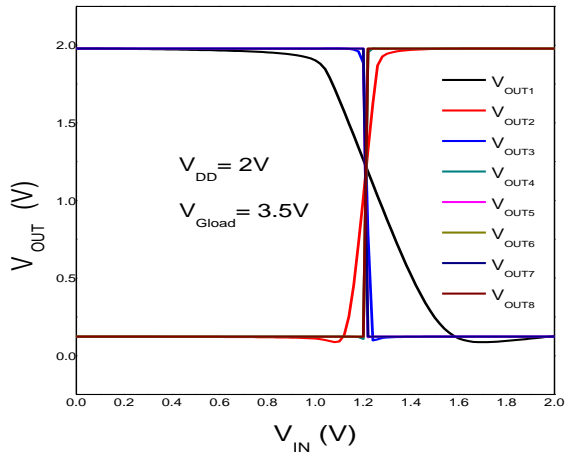


Fig. 10: Transfer Characteristics of a 9-stage ring oscillator depicting intermediate outputs of the cascaded stages.

4. Conclusion

To simulate and optimize vertical JLNT-based logic circuit performance, the circuit design should be based on compact models, i.e. JLNTs, interconnects, resistances and capacitances. Therefore, it is mandatory to develop computationally efficient Verilog-A codes of the scalable, physics-based compact models of JLNTs (with several geometries and NWs in parallel) including parasitic elements. The

results presented in this paper illustrate the first attempt towards non-conventional logic circuit design. With that in mind, in this work, we report a physics-based SPICE-compatible Verilog-A compact modeling approach for 14 nm gate-all-around vertical junctionless nanowire transistors, validated against extensive measurements on an emerging vertical JLNT technology. Very good model accuracy has been observed over different geometries under study. The compact model has been exploited further for studying the performances of inverter-based transistor logic circuits with active and passive loads, complementary topologies as well as a 9-stage ring oscillator. Perspectives are discussed for exploring the proposed modeling framework in innovative 3D logic cell design in order to develop energy-efficient hardware for future high-performance computing paradigms.

Acknowledgement

This work was supported by the LEGO project (Grant ANR-18-CE24-0005-01) and by the project FVLLMONTI funded by European Union's Horizon 2020 research and innovation program under grant agreement N°101016776.

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