A cost-effective technology to improve power performance of nanoribbons GaN HEMTs

Ali Soltani, Brahim Benbakhti, J.-C. Gerbedoen, Abdelkrim Khediri, Maher, Hassan, Jean-Paul Salvestrini, Abdallah Ougazzaden, Nour Eddine Bourzgui, Hassan Ali Barkad

A Cost-Effective Technology to Improve Power Performance of Nanoribbons GaN HEMTs

A. Soltani[1,2], B. Benbakhti[3], J-C Gerbedoen[4], A. Khediri[5], H. Maher[2], J-P Salvestrini[6], A. Ougazzaden[6], N. E. Bourzgui[1], H. A. Barkad[7]

[1]*IEMN/CNRS 8520, Cité Scientifique, Avenue Poincaré, Villeneuve d'Ascq 59651, France*
[2]*LN2, CNRS-IRI-3463, 3IT, Université de Sherbrooke, 3000 Bd de l'Université, Sherbrooke, J1K0A5, QC-Canada*
[3]*School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K. (corresponding author: b.benbakhti@ljmu.ac.uk)*
[4]*LIMMS/CNRS-IIS, UMI 2820, The University of Tokyo, Lille, France*
[5]*Laboratoire de Microélectronique Appliquée, Université Djillali Liabès de Sidi Bel Abbès, 22000, Algeria*
[6]*UMI 2958 CNRS, Georgia Institute of Technology, GT-Lorraine, 57070 Metz, France*
[7]*Institut Universitaire de Technologie Industrielle, Université de Djibouti, BP 1904 Djibouti, Djibouti*

A cost-effective fabrication process is developed to improve the power performance of AlGaN/GaN High Electron Mobility Transistors (HEMTs). This process uses nitrogen ion (N^+) implantation to form multiple parallel NanoRibbons on AlGaN/GaN heterostructures, with thin buffer layer (AlGaN/GaN NR-HEMTs). SRIM simulations of the N^+ implantation combined with measured current-field characteristics reveal a good electrical isolation beneath the 2-dimensional electron gas (2DEG), resulting in substantial increase of the breakdown field of the NR-HEMTs, when compared to conventional AlGaN/GaN HEMTs. The fabricated AlGaN/GaN NR-HEMTs performed (i) an ON/OFF current ratio more than two orders of magnitude larger and (ii) a buffer leakage current more than one order of magnitude weaker than that of the conventional AlGaN/GaN HEMTs. The on-resistance, R_{ON}, and series resistance, R_S, of AlGaN/GaN NR-HEMTs are both reduced by one order of magnitude, when compared to those of the conventional AlGaN/GaN HEMTs. These have boosted the drive current density by up to 435%. Furthermore, we have found that the architecture of the AlGaN/GaN NR-HEMTs reduces the destructive impact of electron traps in the device. An optimized AlGaN/GaN NR-HEMT exhibited a better electrostatic integrity, a subthreshold slope of ~210 mV/dec instead of 730 mV/dec for a conventional GaN HEMT. A higher linearity in the transconductance, g_m, of NR-HEMTs is observed, twice of that of a conventional GaN HEMT. These results demonstrate the great interest of developed process technology, of NR-HEMTs, for high-power switching applications.

GaN-based HEMTs are among the most promising candidates for high-power and high-speed electronics[1]. They are attractive for digital electronics and withstanding high-power under high-temperature environments[2,3]. In the last decade, diverse fabrication processes, e.g. carbon doped or thick buffer layers, gate with a field-plate[4,5], MISHEMT structures[6], were investigated and proposed by several research groups to enhance performance of GaN devices[7,8]. Nonetheless, key device limitations such as large buffer leakage currents,[7,4] high on-resistance (R_{ON}),[9] low drain current density, and relatively poor gate control of the 2D channel are still holding back a wider application of GaN HEMTs. In addition, the above mentioned fabrication processes are non-planar and, thus, costly[10]. To overcome these issues, other research groups have proposed and/or attempted to use nano-structured channels like nano-mesa channels (tri-gate) HEMT,[11-14] and nano-strip (NS) channels,[15-17] for power switching and RF applications, respectively. Although, GaN HEMTs with tri-gate have demonstrated an improved gate control, they still suffer from low drain currents, high R_{ON} and nonlinear transconductance (g_m)[13,14]. Consequently, they are very difficult to be integrated in power switching applications. However, InAlN/GaN HEMTs with NS, developed for RF applications, have manifested better linearity performance in both g_m and transition frequency (f_T) when compared to conventional and tri-gate HEMTs [15,17].

In this paper, we propose a cost-effective technology to fabricate nanoribbon (NR) channels by N^+ implantation, for AlGaN/GaN HEMTs on Si(111) substrate. The overall aim is to develop a low-cost and a planar GaN device technology for power switching applications. We report on the device fabrication technology and performance assessment of these nanoribbon channel devices, including a low R_{ON}, a linear transconductance, a high drain current, and a good gate-to-channel control.

The epi-layers of the processed AlGaN/GaN HEMTs were grown by MetalOrganic Chemical Vapor Deposition (MOCVD) on Si(111) substrate. As illustrated in Fig.1a, the epi-layers structure consists of a 7 nm thick GaN cap layer, 26 nm thick $Al_{0.25}Ga_{0.75}N$ barrier, 1.5 nm thick AlN spacer and 700 nm thick semi-insulating GaN.

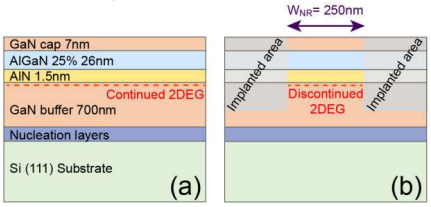


Fig. 1. (a) Schematic cross-section of the HEMT epi-layers grown by MOCVD on Si (111) substrate. (b) Targeted AlGaN/GaN heterojunction nanoribbon, made by N^+ ionic implantation.

A 2-dimensional electron gas (2DEG) sheet carrier density, N_S, of 9.7×10^{12} cm^{-2}, an electron mobility, μ_n, of 1700 $cm^2/V.s$, and a sheet resistance, $R_{\square}$, of 381 Ω/□ were determined by Hall effect measurements at room temperature on the as-grown wafer. The length (L_{NR}) and width (W_{NR}) of the targeted NR, highlighted in Fig. 1b, are 2 µm and 250 nm, respectively. The spacing between nanoribbons is 750 nm.

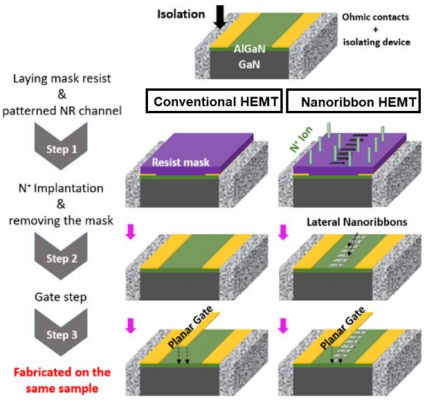


Fig. 2. Fabrication process flow of the conventional AlGaN/GaN HEMT (left panel) and of the nanoribbon (NR) AlGaN/GaN HEMT (right panel). Both conventional and NR HEMTs are fabricated on the same wafer.

The proposed process flow of the device fabrication is summarized in Fig. 2. First, ohmic contacts with Ti/Al/Ni/Au (12/200/40/100 nm) metallization scheme were formed and annealed at 850 °C for 30 s in N_2 atmosphere. The mesa isolation was then defined by N^+ multiple implantations based on different doses and energies. The source/drain contact resistance determined by Transmission Line Model (TLM) measurement is 0.37 Ω.mm. Next, a 300 nm thick CSAR 62 resist layer was deposited and patterned by electron beam lithography (e-beam), using AR 600-546 developer. This is to form mask openings for the subsequent N^+ ion implantation, allowing for the isolation of the 2DEG and formation of NR channels. To process the gate terminal, the CSAR 62 resist mask was afterward removed, and the gate pattern was defined by the e-beam of PMMA 4% 950K resist. Thereafter, Ni/Au (40/300 nm) metal deposition was performed featuring e-beam exposure and evaporation and annealed at 450°C for 20 min. Finally, the samples were passivated by SiN/SiO_2 (50/100 nm) multilayers using PECVD.

TABLE I. Implantation energies and N^+ doses for each sample

Samples	Ion implantation energy (keV)	Dose of implanted N^+ ($\times 10^{14}$ at/cm^2)
Sample A	20 & 30	0.25 & 1.0
Sample B	20 & 40	0.25 & 1.0
Sample C	20 & 50	0.25 & 1.0

To examine the effect of the N^+ ion energy on the quality of the isolation, three samples (A, B and C) are considered. All samples are implanted twice. During the first N^+ implantation, an energy of 20 keV is used for all samples. Then, different ion energies of 30 keV, 40 keV and 50 keV are used throughout the second implantation for the samples A, B and C, respectively. All implantation energies have been limited to 50 keV to avoid any polymerization of the resist mask. The implantation conditions are optimized using SRIM software. Table 1 summarizes the implantation energies and the corresponding doses for each sample.

Fig. 3 shows the simulated 2D distribution of the Nitrogen vacancy concentration, induced by the N^+ implantation, for the three samples. Intensifying the implantation energy leads (i) to an increase of the isolation depth from 120 nm up to 180 nm and (ii) to a lowering of the NR width from 120 nm down to 65 nm. It is important to note that this device fabrication process is a cost effective technology since:

- nano-metric channels width are achieved by using a photolithography, not by an e-beam,
- it uses relatively low implantation energies and doses, less than 50keV and 1×10^{14} at/cm^2,
- it forms an effective electrical isolation beneath the 2DEG channels,
- it does not require thick buffer layer and/or high quality of substrate.

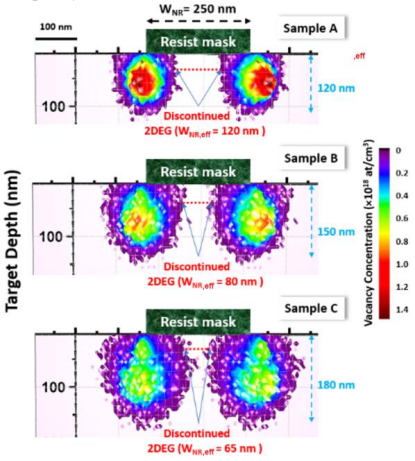


Fig. 3. Impact of the implantation energies on the isolation depth into the epi-layer and on the effective width of 2DEG. These SRIM simulation results demonstrate the efficiency of the ion implantation to (i) achieve a nano-metric channel width using optical lithography and (ii) to isolate the area beneath the 2DEG.

In order (i) to evaluate the efficiency of N^+ implantation on the isolation and (ii) to validate experimentally the optimized implantation energies, summarized in Table I, two TLM structures are designed and then fabricated. The breakdown electric fields of these structures are later measured and compared. The first TLM, implemented to check the quality of the isolation, consists of two 100 µm wide ohmic contacts separated by a distance of 10 µm. The active area between the two ohmic electrodes of this TLM is isolated by N^+

implantation with multiple energies of 20, 50, 100 and 150 keV, and doses of 0.25, 1, 1.5, 2.5 × 10^{14} at/cm^2, respectively. The second TLM, designed to validate the optimized implantation conditions, has the same width and length as the first TLM. However, an interdigital fingers (IF) pattern, very similar to the NRs used in the GaN HEMTs, are fabricated in between the ohmic electrodes (see inset of Fig. 4). The space between the interdigital fingers is N^+ implanted with the energies and doses presented in Table 1.

Fig. 4 presents the measured current-electric field characteristics of the first TLM (without IF) and the second TLM (with IF for the three samples). It is noted that the breakdown electric field increases as the implantation energy increases in the second TLM structure. It varies from 0.9 MV/cm to 1.35 MV/cm, and 1.64 MV/cm at a current of 1 µA for the sample A, B, and C, respectively. As previously described, using small openings and, even with relatively low N^+ implantation energies and doses (less 50 keV and 1×10^{14} at/cm^2), lead to a deeper material isolation and, thus, higher breakdown electric fields. For large openings, e.g. the first TLM, even a high implantation energy of 150 keV is not sufficient to reach a depth into the epi-layer. This explains the relatively low breakdown field of 0.35 MV/cm measured in the first TLM (without IF).

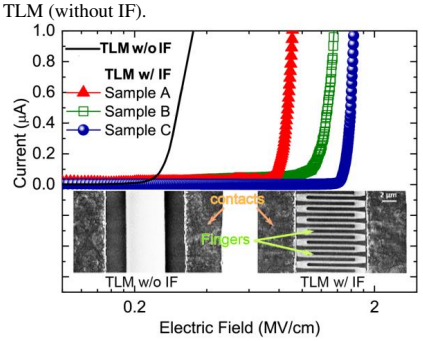


Fig. 4. Current-Electric field characteristics of the TLM without interdigital fingers (IF) and with IF (samples A, B, and C). Inset shows the top-view SEM images of the TLM with and without interdigital fingers.

Afterwards, two types of transistor are fabricated, (i) conventional HEMT without NRs (ref-HEMT) and (ii) NR-HEMTs using the optimized N^+ implantation energies and doses. The top views of these transistors, obtained by Scanning Electron Microscope (SEM), are shown in Fig. 5.

The DC output characteristics of the conventional HEMT, used as a reference, and of the NR-HEMTs are compared in Fig. 6a. For the NR-HEMTs, the DC current density are normalized by the effective channel width ($W_{eff} = W_{NR} \times N_{NR}$, where W_{NR} is the NR width and N_{NR} is the total number of NRs). This is to allow a comparison of the intrinsic device performance.

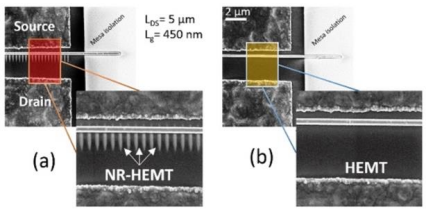


Fig. 5. Top view SEM images of (a) the AlGaN/GaN NR-HEMT and (b) conventional AlGaN/GaN HEMT. The length and width of NR are 2 µm and 250 nm, respectively. The gate length and source-to-drain spacing are 450 nm and 5 µm, respectively.

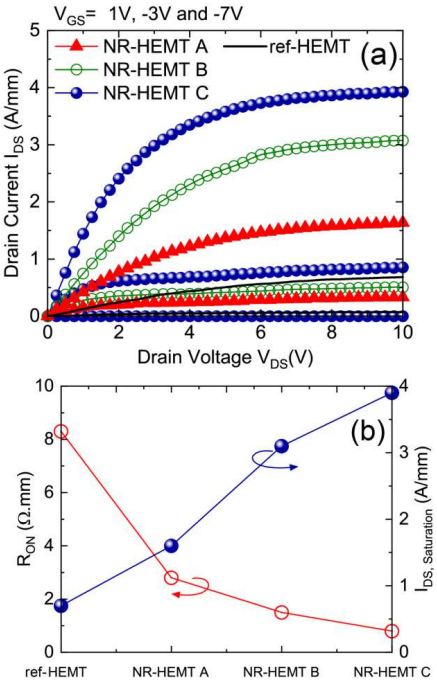


Fig. 6. (a) I_{DS}-V_{DS} DC output characteristic of the fabricated conventional and NR AlGaN/GaN HEMTs. V_{DS} sweeping is from 0V to 10 V and V_{GS} values are for 1 V, -3 V and -7 V. (b) The extracted values of the on-resistance, R_{ON}, and the drain saturation current, $I_{DS, Satutration}$.

The output current density of the optimized NR-HEMT (NR-HEMT C) is much larger than that of the conventional HEMT. For example, at V_{DS}= 10 V; V_{GS} = 1 V, the maximum current density, $I_{D,Saturation}$, for NR-HEMT C is as high as 3.9 A/mm, which is approx. ~460% higher than 0.7 A/mm obtained for the conventional HEMT (Fig. 6b). This is consistent with the expectation that the NR-HEMT structures have better themal management and higher current control

when compared to the conventional HEMTs[15-19]. The R_{ON} of the conventional HEMT and NR-HEMTs A, B, and C at V_{GS}= 0 V, extracted from I_{DS}-V_{DS} sweeps in the linear region (Fig. 6b), are 8.3, 2.8, 1.5 and 0.8 Ω.mm, respectively. The NR-HEMT has demonstrated a much smaller R_{ON}, in contrast to the conventional HEMT.

All NR-HEMT samples have clearly demonstrated improved off-current (I_{OFF}) and better linearity in the transconductance, g_m, as shown in Fig. 7. The NR-HEMT C features a reduction in I_{OFF} of ~2 orders of magnitude compared to the conventional HEMT, revealing a lower charge trapping effect. The higher linearity in g_m of NR channel devices validates the reported mechanism described in[16]. In conventional HEMT, the extrinsic g_m drops quickly when increasing the drain current after reaching its peak value, and this issue becomes more important as the gate length scales down. Several theories were proposed over the years to explain this behavior. Palacios *et al.*[20], DiSanto *et al.*[21], and Trew *et al.*[22] correlate this behavior with the increase of the source access resistance, R_S, and showed that intrinsic devices without the access resistance can have a flat g_m.

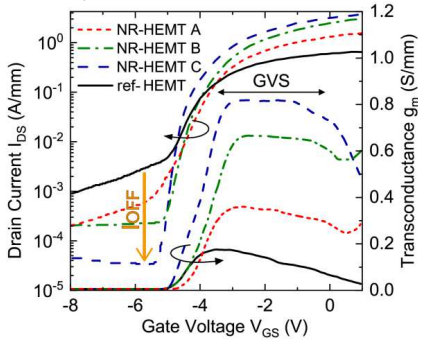


Fig. 7. I_{DS}-V_{GS} and transconductance, g_m, transfer characteristics of the fabricated conventional HEMT and NR-HEMTs, measured at the drain bias V_{DS}= 8 V.

To quantitatively evaluate the linearity performance of the different samples, a figure of merit namely gate-voltage-swing (GVS) is derived. It is based on the gate voltage range, where a device parameter, i.e. g_m, stays larger than 80% of its maximum value[23]. The corresponding GVS values of the conventional HEMT device is 2 V (from −4 to −2 V). The NR-HEMT C device shows a better linearity of GVS = 4 V (from −3.5 to 0.5 V).

The measured source resistance, R_S, as a function of gate current, I_{GS}, for the different samples is shown in Fig. 8. The measurement setup adopts the gate current injection method[24,25], as illustrated in the inset of Fig. 8. Initially, as I_{GS} increases from 0.01 mA/mm up to I_{GS} ≃ 1 mA/mm, R_S values of all samples drop down rapidly. For $I_{GS} \geq 1$ mA/mm, the decline of R_S diminish to reach constant values at $I_{GS} \simeq 10$ mA/mm of about 2, 0.8, 0.4, and 0.25 Ω.mm, respectively. The NR-HEMTs have lower R_S than that of the conventional HEMT.

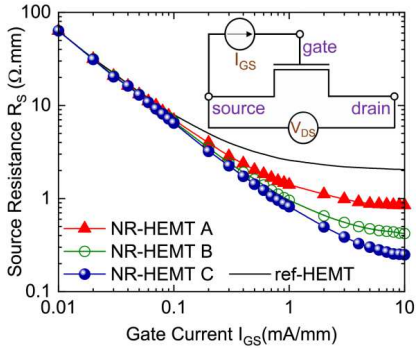


Fig. 8. R_S-I_{GS} transfer characteristics of the investigated NR-HEMTs and conventional HEMT. The inset illustrates the used gate-current-injection technique.

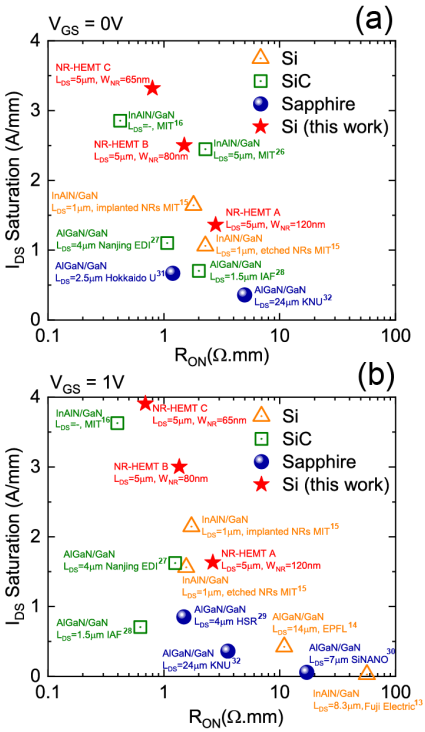


Fig. 9. Summary on the static on-resistance, R_{on}, and on the saturation current, I_{sat}, of state-of-the-art AlGaN/GaN NR-HEMTs. (a) V_{GS}=0V, (b) V_{GS}=1V.

Since the on-state performance of the NR-HEMTs can be affected by the involved isolation technique, both R_{ON} and saturation current $I_{DS,\ Saturation}$ of our fabricated NR-HEMTs (A, B and C) are benchmarked against the state-of-the-art of GaN NR-HEMTs in Fig. 9. The NR-HEMT C performs a low R_{ON} of 0.8 and 0.7 Ω.mm at V_{GS}= 0 V and V_{GS}= 1 V, respectively. This is the lowest R_{ON} for NR-HEMTs (In,Ga)AlN/GaN on a silicon substrate. The R_{ON} for all referenced[13-16,26-32] devices were extracted and/or re-calculated based on the reported data.

The key DC parameters of both NR-HEMTs and conventional HEMT, are extracted and given in Table II. Usually, the smaller the subthreshold slope (SS) is, the higher the off-state performance of the device will be. Conventional HEMT features a SS of 730 mV/decade, while NR-HEMT exhibits a much lower value of 210 mV/decade. This demonstrates a better off-state performance of NR-HEMT. The SS values of the other NR-HEMT samples are lower than those of conventional HEMTs, divulging a reduced electron trapping effect and an enhancement of the gate control capability.

TABLE II. The main DC characteristics of the benchmarked devices (A, B and C) versus the conventional HEMT.

	Ref HEMT	NR-HEMTs		
		A	**B**	**C**
I_{max} (A/mm) @ V_{GS} = 0 V	0.62	1.62	2.47	3.32
R_{on} (Ω.mm) @ V_{GS} = 0 V	8.3	2.8	1.5	0.8
V_{th} (V) @ 1 mA/mm	-7.5	-5.3	-4.8	-4.9
SS (mV/dec)	730	714	368	210
ON/OFF ratio	6×10^2	6×10^3	10^4	10^5
Peak g_m (S/mm)	0.17	0.36	0.66	0.82
Figure of merit GVS [a] (V)	2	3.5	3.7	4

[a]Gate-Voltage-Swing (GVS), where the device parameter remains ≥80% of its maximum value.

The threshold voltage (V_{th}) of the conventional HEMT is about −7.5 V. However, NR-HEMTs have reduced V_{th} of about −5.3, −4.8, −4.9 V, respectively. This positive shift of V_{th}, in respect to the V_{th} of the conventional HEMT, is the consequence of decreased active area in NR-HEMTs due to the N^+ implantation, diminution of the effective 2DEG concentration. All V_{th} values are extracted by a constant-current method, which was defined as the gate voltage where the drain current reached 1 mA/mm.

In summary, a low-cost process technology, based on N^+ implantation of nanoribbons and thin GaN buffer layer, has been developed for AlGaN/GaN HEMTs. The N^+ implantation conditions, energy and dose, have been simulated/optimized and then evaluated/validated experimentally. We demonstrated that a successive implantations, with low energies of 20 keV followed by 50 keV, leads to an excellent isolation of the area below the 2DEG channel. A nano-metric channel width of 65 nm has been achieved by using the photolithography, a cost effective process. As results, a much higher breakdown field has been observed for the NR-HEMTs when compared to conventional AlGaN/GaN HEMT.

The fabricated/optimized AlGaN/GaN NR-HEMT has shown an ON/OFF current ratio more than two orders of magnitude larger, ∼2 orders of magnitude lower I_{OFF} current. The R_{ON} value of this NR-HEMT at V_{GS}= 1 V is as low as 0.7 Ω.mm, around 10 times lower than that of the conventional AlGaN/GaN HEMT. These enhanced static properties have resulted in AlGaN/GaN NR-HEMT with ∼163–435% higher drain current density than that of conventional HEMTs. We found that the optimized process has led to (i) improving the linearity of the transconductance g_m, (ii) lowering the R_S and (iii) steepening the subthreshold slope of the AlGaN/GaN NR-HEMT. Overall, the results indicate that nanoribbon channels structure fabricated by nitrogen ions implantation can be a favorable way to manufacture devices for high-power switching application.

Acknowledgment

This work has been supported by GANEX (a public funded 'Investissements d'Avenir' program managed by the French ANR agency), by the French council region of Lorraine "Region Lorraine" and by the ANR project Cleaning ANR- 15-CE09-0019**.**

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

[1]S. Yoshida, J. Li, T. Wada, and H. Takehara, in *ISPSD '03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, 2003. Proceedings.* (IEEE, Cambridge, UK, 2003), pp. 58–61.

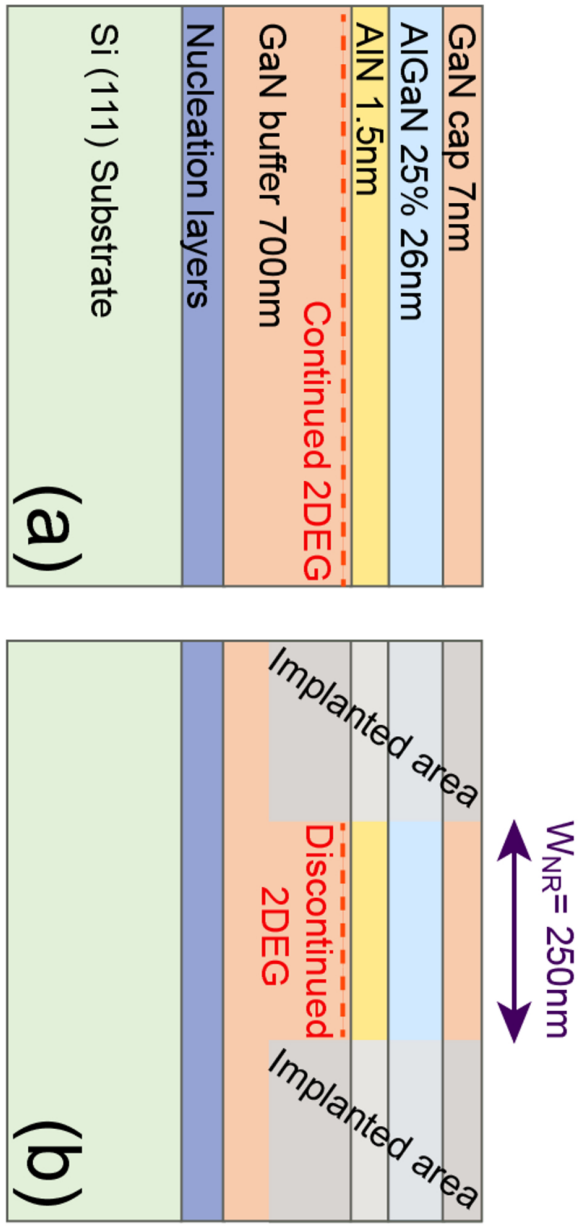
[2]G. Tang, A.M. Kwan, R.K. Wong, J. Lei, R.Y. Su, F.W. Yao, Y.M. Lin, J.L. Yu, T. Tsai, and H.C. Tuan, IEEE Electron Device Letters **38**, 1282 (2017).

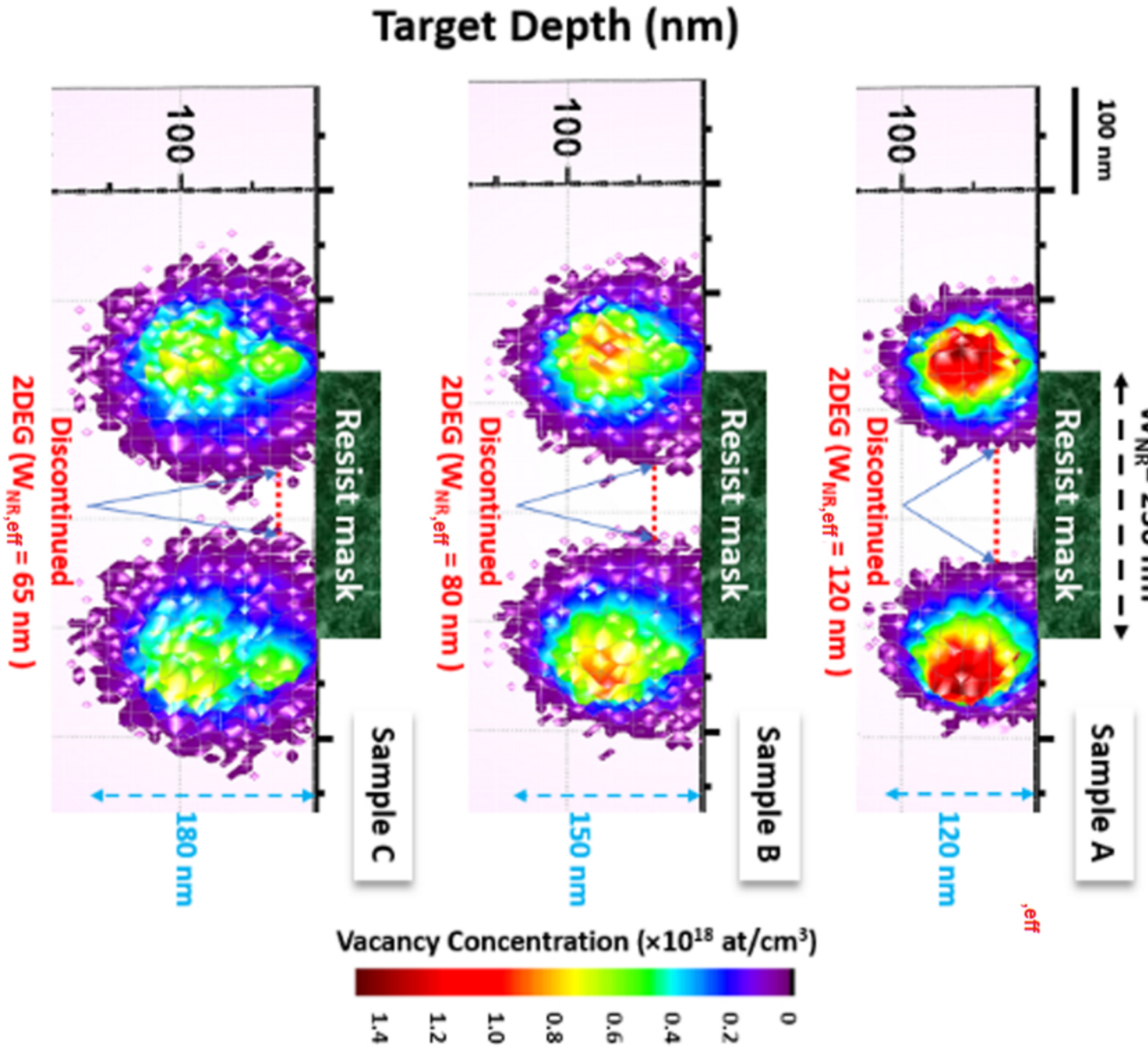
[3]Z. Xu, J. Wang, Y. Cai, J. Liu, Z. Yang, X. Li, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, and Y. Hao, IEEE Electron Device Letters **35**, 33 (2014).

[4]W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, IEEE Electron Device Letters **29**, 8 (2008).

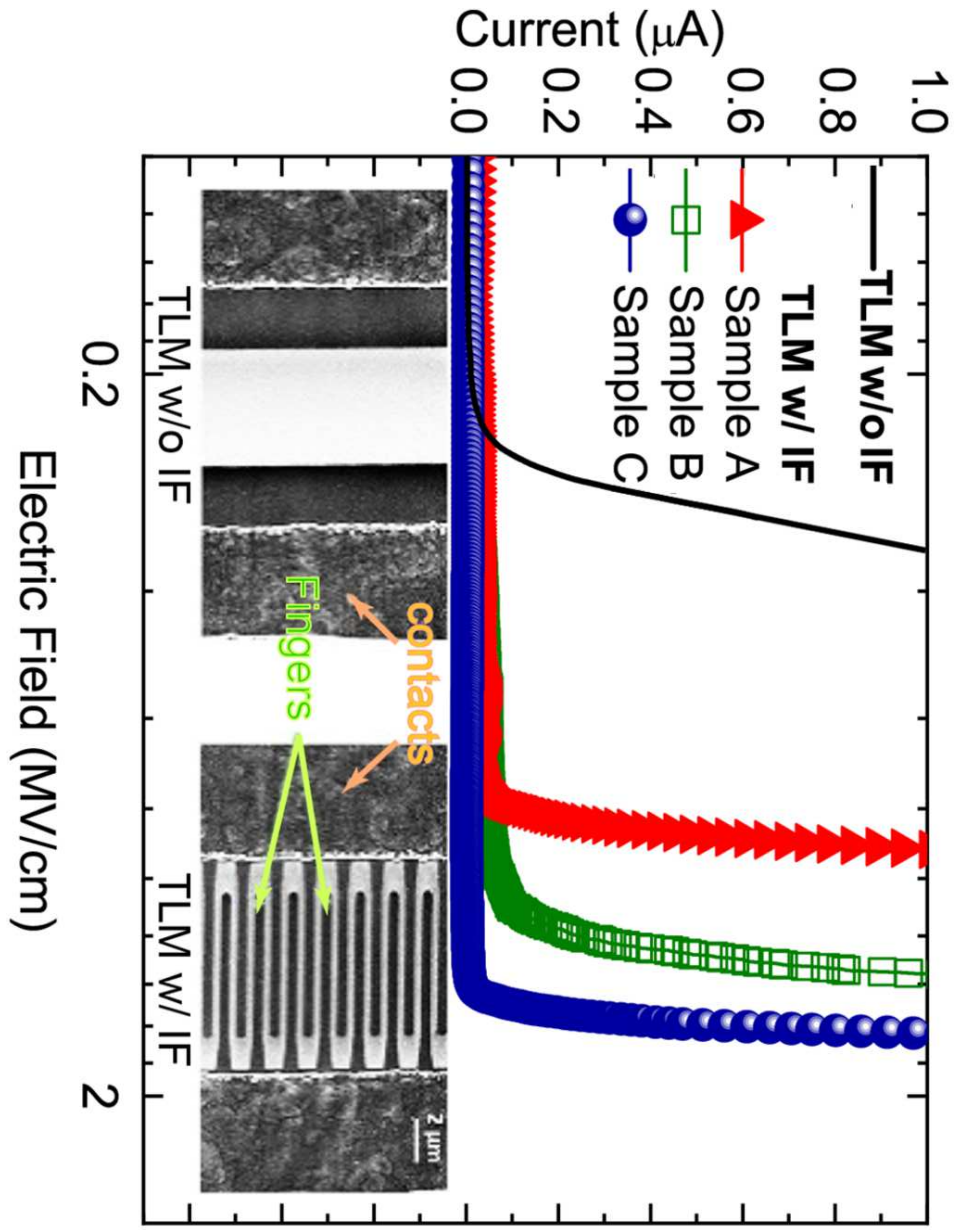
[5]Rongming Chu, A. Corrion, M. Chen, Ray Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, IEEE Electron Device Letters **32**, 632 (2011).

[6]M. Van Hove, S. Boulay, S.R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere, IEEE Electron Device Letters **33**, 667 (2012).
[7]N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, and S. Yoshida, Proceedings of the IEEE **98**, 1151 (2010).
[8]Y. Cai, Y. Zhou, K.M. Lau, and K.J. Chen, IEEE Transactions on Electron Devices **53**, 2207 (2006).
[9]W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, IEEE Transactions on Electron Devices **54**, 1825 (2007).
[10]I.B. Rowena, S.L. Selvaraj, and T. Egawa, IEEE Electron Device Letters **32**, 1534 (2011).
[11]B. Lu, E. Matioli, and T. Palacios, IEEE Electron Device Letters **33**, 360 (2012).
[12]K. Ohi and T. Hashizume, Jpn. J. Appl. Phys. **48**, 081002 (2009).
[13]S. Takashima, Z. Li, and T.P. Chow, IEEE Transactions on Electron Devices **60**, 3025 (2013).
[14]J. Ma and E. Matioli, IEEE Electron Device Letters **38**, 367 (2017).
[15]W. Xing, Z. Liu, H. Qiu, G.I. Ng, and T. Palacios, IEEE Electron Device Letters **38**, 619 (2017).
[16]D.S. Lee, H. Wang, A. Hsu, M. Azize, O. Laboutin, Y. Cao, J.W. Johnson, E. Beam, A. Ketterson, M.L. Schuette, P. Saunier, and T. Palacios, IEEE Electron Device Letters **34**, 969 (2013).
[17]W. Xing, Z. Liu, K. Ranjan, G.I. Ng, and T. Palacios, IEEE Electron Device Letters **39**, 947 (2018).
[18]Benbakhti, M. Rousseau, A. Soltani, J. C. De Jaeger, IEEE Transactions on Electron Devices **53**, 2237 (2006).
[19]Benbakhti, A. Soltani, K. Kalna, M. Rousseau, J. C. De Jaeger, IEEE Transactions on Electron Devices **56**, 2178 (2009).
[20]T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, and U.K. Mishra, IEEE Transactions on Electron Devices **52**, 2117 (2005).
[21]D.W. DiSanto and C.R. Bolognesi, IEEE Transactions on Electron Devices **53**, 2914 (2006).
[22]R.J. Trew, Yueying Liu, L. Bilbro, Weiwei Kuang, R. Vetury, and J.B. Shealy, IEEE Transactions on Microwave Theory and Techniques **54**, 2061 (2006).
[23]Z.H. Liu, G.I. Ng, S. Arulkumaran, Y.K.T. Maung, K.L. Teo, S.C. Foo, and S. Vicknesh, in *The 5th European Microwave Integrated Circuits Conference* (2010), pp. 41–44.
[24]D.R. Greenberg, IEEE TRANSACTIONS ON ELECTRON DEVICES **43**, 3 (1996).
[25]D.R. Greenberg and R. Bhat, 9 (n.d.).
[26]M. Azize, A.L. Hsu, O.I. Saadat, M. Smith, X. Gao, S. Guo, S. Gradecak, and T. Palacios, IEEE Electron Device Letters **32**, 1680 (2011).
[27]K. Zhang, Y. Kong, G. Zhu, J. Zhou, X. Yu, C. Kong, Z. Li, and T. Chen, IEEE Electron Device Letters **38**, 615 (2017).
[28]E. Ture, P. Bruckner, R. Quay, O. Ambacher, M. Alsharef, R. Granzner, and F. Schwierz, in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)* (IEEE, London, United Kingdom, 2016), pp. 61–64.
[29]X. Zhou, X. Tan, Y. Lv, Y. Wang, X. Song, G. Gu, P. Xu, H. Guo, Z. Feng, and S. Cai, IEEE Transactions on Electron Devices **65**, 928 (2018).
[30]S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K.J. Chen, and B. Zhang, IEEE Electron Device Letters **33**, 354 (2012).
[31]K. Ohi, J.T. Asubar, K. Nishiguchi, and T. Hashizume, IEEE Transactions on Electron Devices **60**, 2997 (2013).
[32]Y.-W. Jo, D.-H. Son, C.-H. Won, K.-S. Im, J.H. Seo, I.M. Kang, and J.-H. Lee, IEEE Electron Device Letters **36**, 1008 (2015).

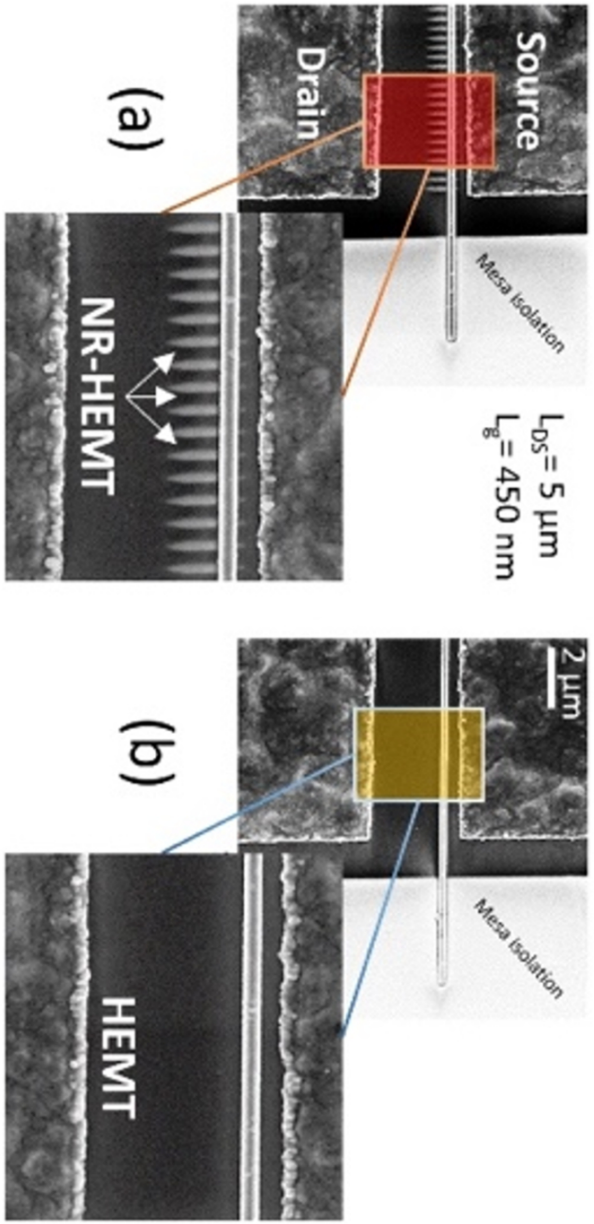


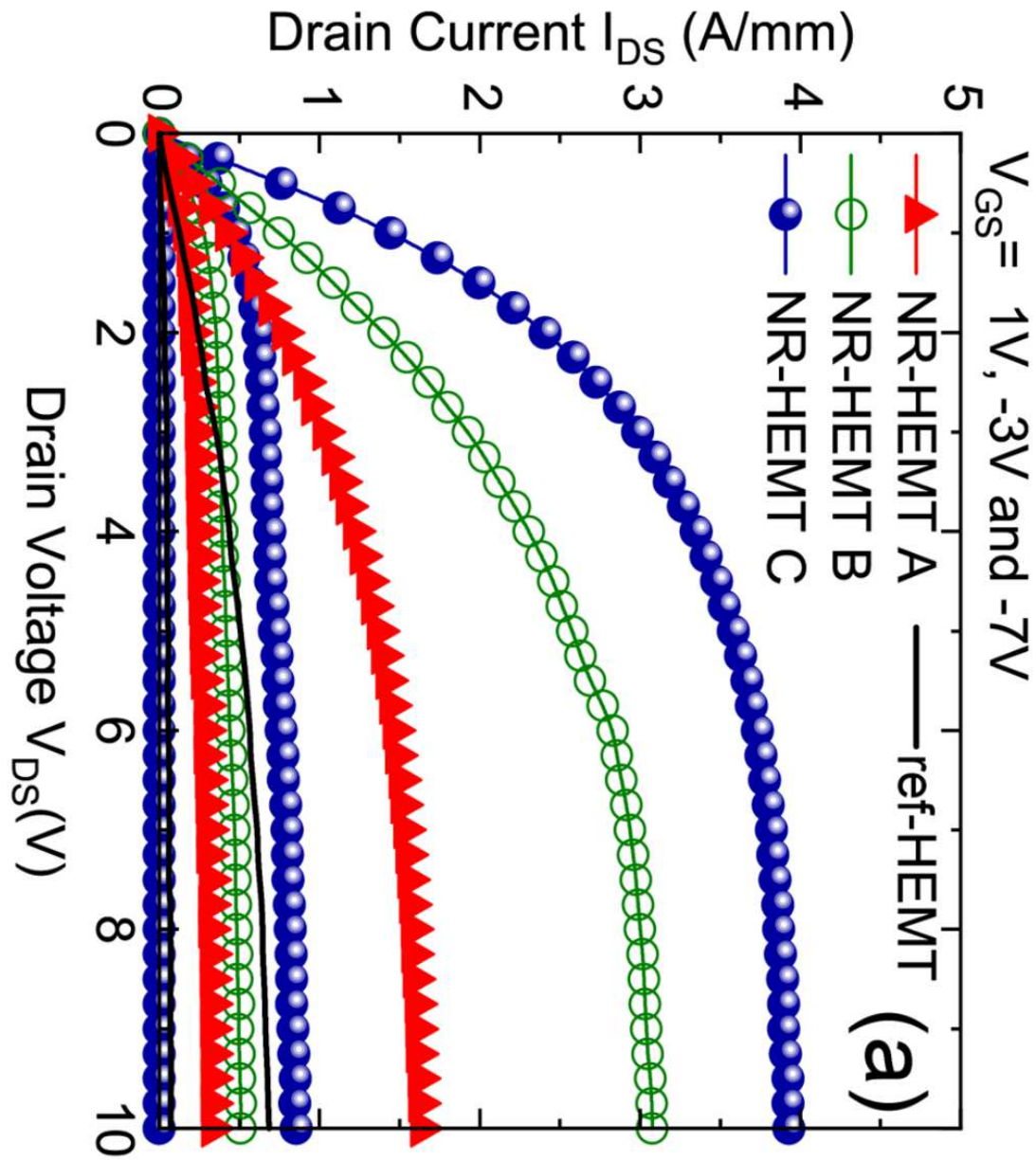


PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0080240

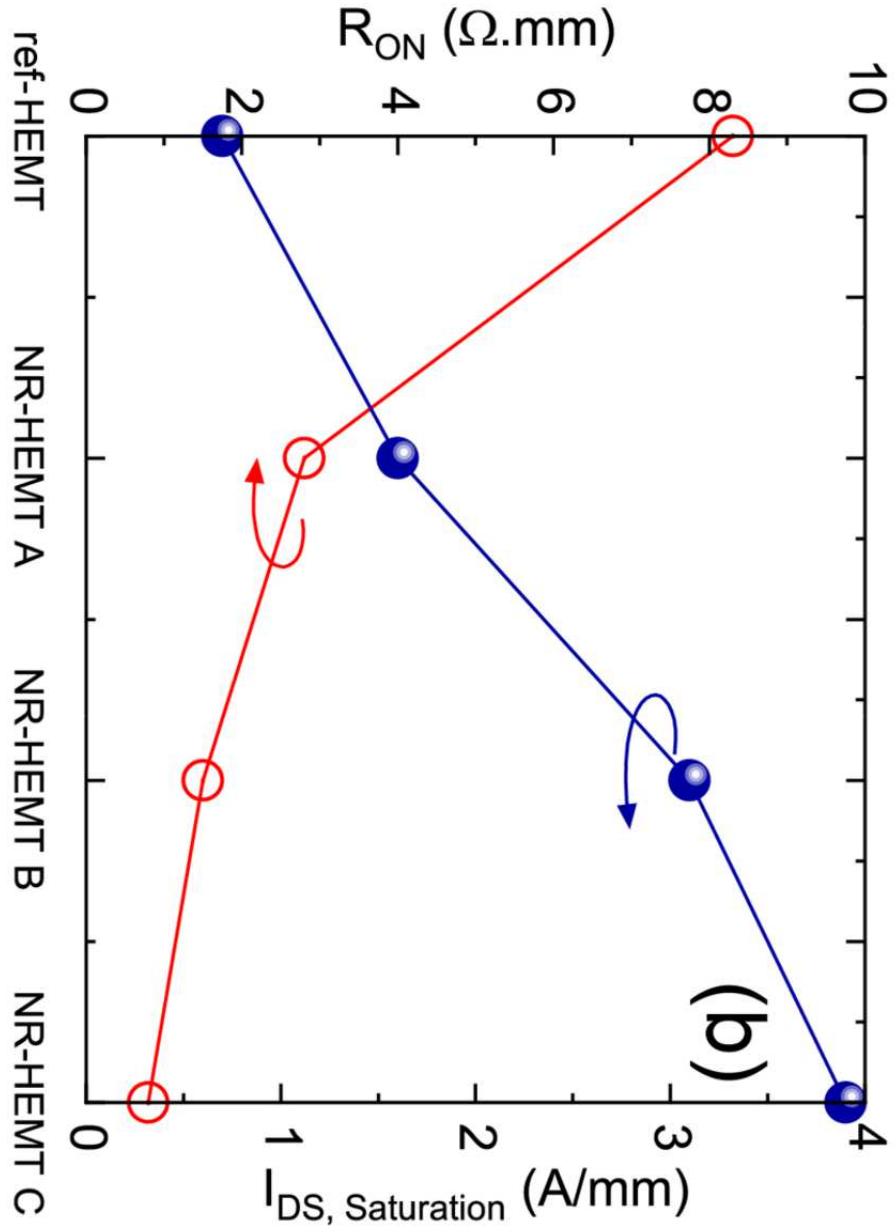


PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0080240

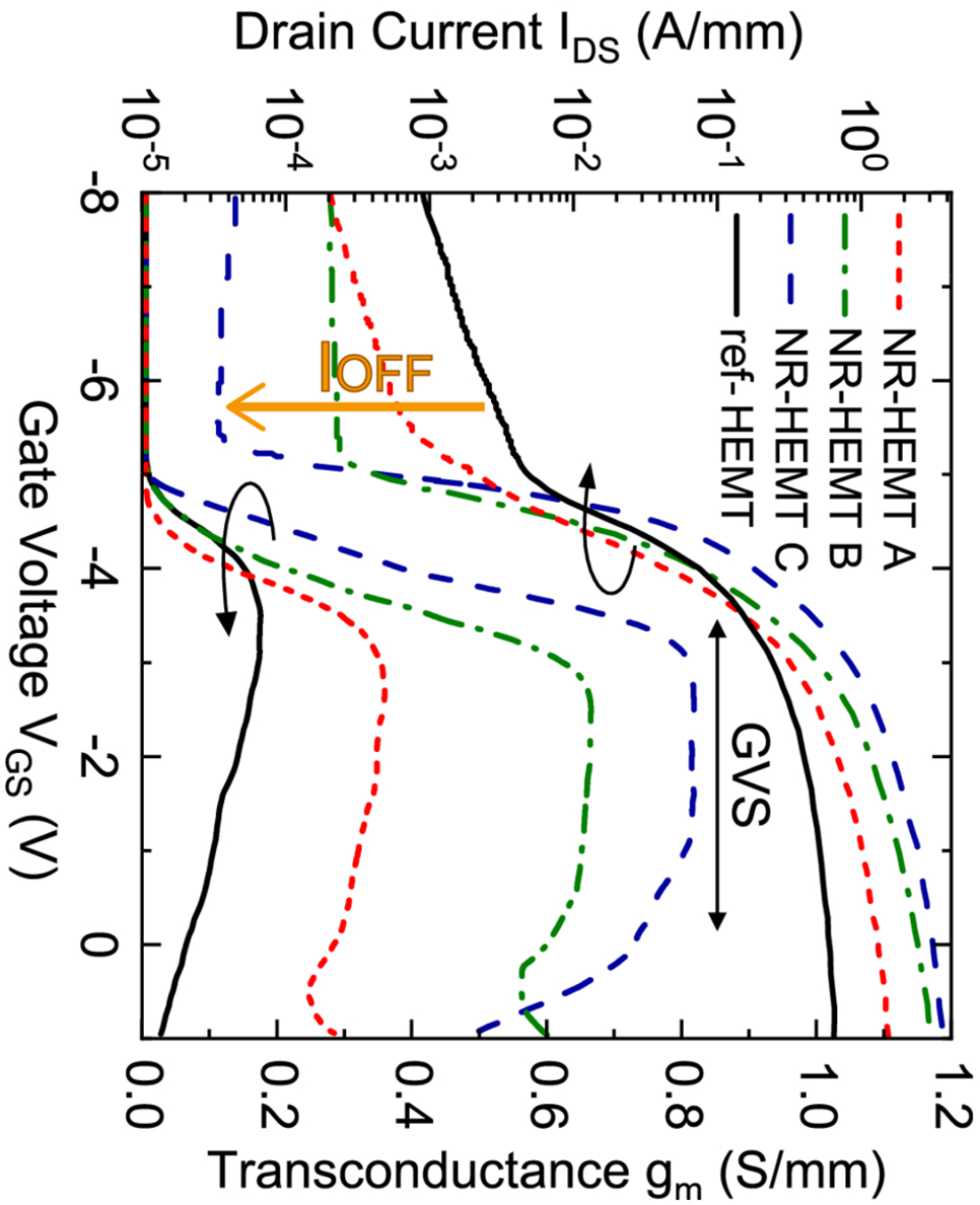




PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0080240



PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0080240



PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0080240