

Large-Scale Monolithic Fabrication of III–V Vertical Nanowires on a Standard Si(100) Microelectronic Substrate

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Article

Large-Scale Monolithic Fabrication of III−V Vertical Nanowires on a Standard Si(100) Microelectronic Substrate

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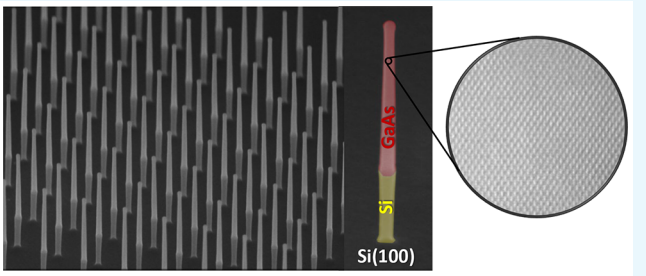
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ABSTRACT: Vertical III−V nanowires are of great interest for a large number of applications, but their integration still suffers from manufacturing difficulties of these one-dimensional nanostructures on the standard Si(100) microelectronic platform at a large scale. Here, a top-down approach based on the structure of a thin III−V epitaxial layer on Si was proposed to obtain monolithic GaAs or GaSb nanowires as well as GaAs−Si nanowires with an axial heterostructure. Based on a few complementary metal−oxide−semiconductor-compatible fabrication steps, III−V nanowires with a high crystalline quality as well as a uniform diameter (30 nm), morphology, positioning, and orientation were fabricated. In addition, the patterning control of nanowires at the nanoscale was thoroughly characterized by structural and chemical analyses to finely tune the key process parameters. To properly control the morphology of the nanowires during reactive-ion etching (RIE), the balance between the plasma properties and the formation of a protective layer on the nanowire sidewall was studied in detail. Furthermore, high-resolution microscopy analyses were performed to gain a better understanding of the protective layer's composition and to observe the crystalline quality of the nanowires. This approach paves the way for the possible scale-up integration of III−V-based nanowire devices with conventional Si/complementary metal−oxide−semiconductor technology.



INTRODUCTION

In the semiconductor world, III−V materials are complementary to silicon (Si). Their exceptional electronic mobilities and direct band gap properties make them attractive in a large spectrum of applications like nanoelectronics,[1,2] nanophotonics,[3,4] biological sensing,[5] photovoltaics,[6,7] and optoelectronics.[8−10] All of these applications greatly benefit from integration with a III−V-nanostructured layer, in particular vertical nanowires.[11,12] Their one-dimensional geometry (large surface-to-volume ratio) and their ability to create heterostructures (axial and radial) offer advantages in terms of their integration and compatibility with conventional microfabrication facilities. However, Si has been and will continue to be the most appropriate platform for the mass production of electronic devices due to its abundance, robustness, and high-quality oxide (SiO_2) as well as the accumulated knowledge around this material and related technologies over the past 50 years. In this study, the cointegration of III−V devices with Si-complementary metal−oxide−semiconductor electronics is proposed to advance the design of new systems that combine the advantages of III−V and Si.

However, the integration of a III−V nanostructure on a Si(100) substrate, the industry-standard Si platform, represents an important challenge to obtain III−V nanowires with a low crystal defect density that are localized and oriented with high precision. For monolithic integration, direct epitaxy of III−V materials on Si(100) is required. One of the key difficulties to epitaxial approaches is to overcome material defects stemming from the crystal lattice mismatch with Si.[13] Moreover, the localization and orientation of III−V nanowires on Si are essential for device integration. The most popular methods to obtain localized III−V nanowires on Si are based on a bottom-up approach, with selective area epitaxy, where the III−V nanostructures are grown selectively on a Si substrate, in most cases using a catalyst[14−16] (e.g., the vapor−liquid−solid method). The first demonstration used networks of metallic catalysts patterned by a liftoff process before nanowire growth.[7,13] Later, self-catalyzed approaches were proposed (e.g., Ga droplets are self-localized in a hole matrix structured in a SiO_2 layer).[17,18] The main advantages of bottom-up growth approaches are the crystalline bulk quality and the favorable surface properties of nanowires. Nevertheless, it is still challenging to fabricate nanowires with high reproducibility on all wafer-scale in terms of diameter, morphology, positioning, crystal structure, and dopant concentration. Moreover, nanowires grown in the vertical direction with a

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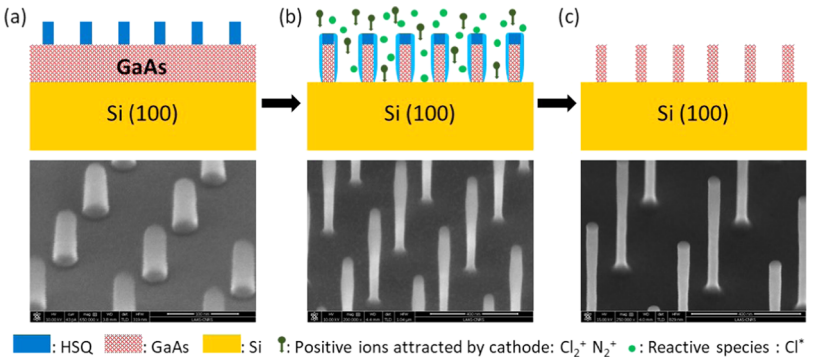


Figure 1. Top-down nano-patterning of vertical GaAs nanowires on a Si(100) substrate (schematic representation and the associated SEM images in a tilted view): (a) nanopatterning of a negative mask by e-beam lithography (HSQ nanopatterns). (b) GaAs plasma etching using Cl_2-based chemistry by tuning the anisotropic etching and the protective layer formation. (c) Stripping of the remaining layers (HSQ resist and sidewall protective layer) by chemical etching.

high yield only have been demonstrated on a Si(111) substrate. Interestingly, the control of the growth direction independently of the substrate orientation has been obtained, thanks to a growth template.[19,20] This method has provided perfectly vertical III−V nanowires on a Si(100) substrate with a low defect density but at the cost of an increase in the process complexity. Additionally, ultimate scaling of the nanowire diameter/pitch is difficult to obtain. Furthermore, the faceting on the top of the nanowire and enlargement of the foot of the structures[20] are issues for device integration, in particular the low resistive contact formation. Finally, very few studies have focused on the patterning of III−V vertical nanowires by a top-down approach with scaled dimensions[21−23] and these have not considered monolithic integration with Si.

Here, we present a wafer-scale approach to fabricate a III−V vertical nanowire array with a low defect density as well as tight control of the location and the diameter on a standard Si(100) microelectronic substrate. This approach is demonstrated on different materials (GaAs and GaSb) and architectures (array of nanowires and array of axial heterostructures). The patterning control of nanowires at the nanoscale was thoroughly studied by structural and chemical analyses by scanning electron microscopy (SEM) and transmission electron microscopy (TEM) coupled to energy-dispersive X-ray spectroscopy (EDX) to understand and tune the key parameters (plasma properties, protective layers, and crystalline properties).

LARGE-SCALE PATTERNING OF A VERTICAL NANOWIRE ARRAY

Our approach is presented in Figure 1, where each step is illustrated with a schematic diagram with the associated SEM images. The vertical III−V nanowires were fabricated using only four standard techniques of micro-/nanofabrication: planar epitaxy of the III−V layer on a Si(100) substrate, nanolithography, plasma etching, and selective chemical stripping.

The starting III−V layer (GaAs and GaSb) was grown by metalorganic chemical vapor deposition on a 300 mm Si(100) substrate with a layer free of antiphase boundaries. Specific Si surface engineering based on annealing creates atomic steps on the Si surface that prevent antiphase boundary formation. The crystalline quality of the epitaxial layer is of prime importance because these crystalline defects degrade the carrier mobility.[24]

Details of the process can be found in references 25, 26. Thicknesses of the III−V layer ranging from 200 to 800 nm were used. First, nanopatterns (Figure 1a) were made by electron beam lithography using a 90 nm negative-tone resist layer, namely, hydrogen silsesquioxane (HSQ), which is a flowable oxide from Dow Corning[27] diluted in methyl isobutyl ketone. To overcome the adhesion issues of small HSQ patterns on a III−V surface, the following surface cleaning protocol was performed prior to HSQ coating: (i) oxygen (O_2) plasma to remove organic residues, (ii) a deoxidation step with 37% HCl mixed with deionized water (DIW) (1:1) for 1 min, (iii) rinsing step with DIW, and (iv) dehydration step on a hot plate at 110 °C for 5 min. The electron beam exposure was carried out with a Raith 150 system at low energy (20 keV) with a base dose of 350 pC/cm a step of 2 nm, and a current of 120 pA. The circular shape was designed using a starlike pattern, composed of lines starting and finishing in the center of the pattern to force the symmetry of the nanopillars and homogeneous distribution of the Gaussian energy.[27] After exposure, the resist was developed by manual immersion in 25% tetramethylammonium hydroxide solution in water to enhance the pattern contrast.[27] A tilted SEM image of an array of HSQ patterns with a diameter of 30 nm, a height of 90 nm, and a pitch of 300 nm is shown in Figure 1a. The following step, illustrated in Figure 1b, is the transfer of nanomasks into the GaAs layer by anisotropic plasma etching. This dry etching is one of the most important modules of the top-down process to reach high aspect ratio and nanometer-scale nanowires with vertical and smooth sidewalls. The key point is the tight engineering of anisotropic etching (the balance between chemical etching and ion bombardment) and protective layer formation on the nanowire sidewall, as depicted in Figure 1b. GaAs nanowires with a vertical sidewall could be achieved with plasma-based-chlorine (Cl_2) chemistry (Figure 1b) down to the Si/GaAs interface. The detection of the etching endpoint was controlled with a laser interferometer to avoid large overetching, which would erode the nanowire base and degrade the mechanical stability of the nanostructures. Finally, the last step was the stripping of the remaining layers (HSQ resist and sidewall protective layer) by chemical etching with 5% hydrofluoric acid (HF) (Figure 1c).

RESULTS AND DISCUSSION

Verticality Control. The diameter and orientation of nanowires are fundamental for device integration. For example,

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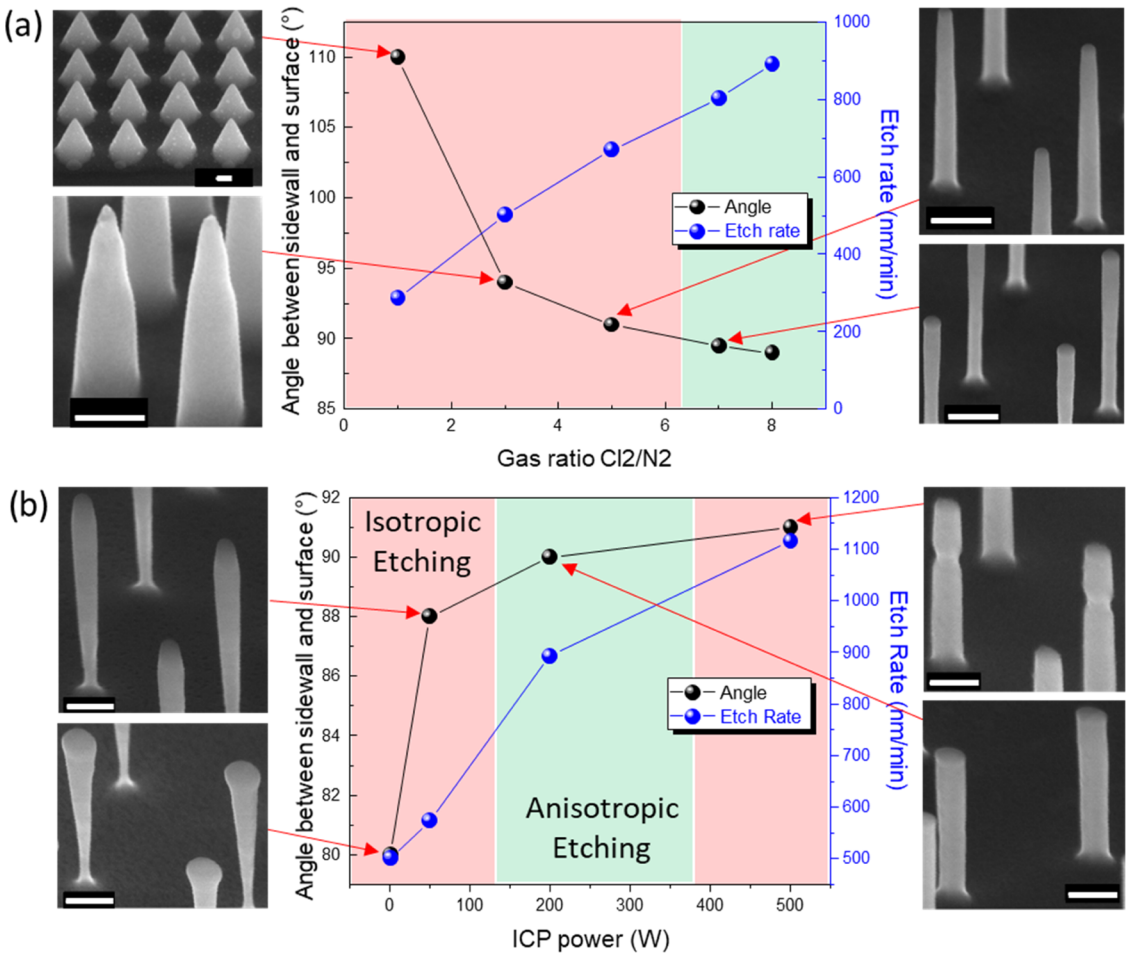


Figure 2. Impact of the plasma parameters on the nanowire sidewall anisotropy and on the GaAs etch rate as well as the related SEM images of the specific conditions (scale bar = 100 nm): (a) Impact of the Cl_2/N_2 gas ratio at Picp = 200 W; Pbias = 60 W; P = 6 mT; and T = 35 °C on nanowire arrays of 60 nm diameter, 600 nm height, and 300 nm space. (b) Impact of the ICP power influence at Cl_2/N_2 = 8; Pbias = 60 W; P = 6 mT; and *T* = 35 °C on nanowire arrays of 40 nm diameter, 600 nm height, and 300 nm space.

gate-all-around transistors[21,22] use nanowires as the conducting channel, and the surface properties or diameter variation can significantly impact the electrical characteristics. Inductively coupled plasma (ICP) reactive-ion etching is the most appropriate system to obtain high-aspect-ratio nanowires with a very low roughness because it allows the gas to be ionized independently of ionic bombardment. Several plasma chemistries can be used to etch GaAs. Generally, chlorine gases are the most suitable to form $GaCl_x$ and $AsCl_x$ volatile products like BCl_3,[31−33] $SiCl_4$,[34] and Cl_2.[29,30,35−38] The current study focused on Cl_2/nitrogen (N_2) chemistry using only chlorine gas,[28] Cl_2, which is less corrosive and dangerous than BCl_3 or $SiCl_4$. As shown in Figure 2, control of the nanostructure geometry by plasma etching was studied by evaluating two key parameters: the gas chemistry (Cl_2/N_2 ratio) and the coil power. Because all of the process parameters are interdependent, the objective was to determine the optimal parameters to obtain a good balance between physical etching (sputtering-related mechanism, mainly anisotropic) and chemical etching (surface reaction-related mechanism, mainly isotropic).

First, to have a better overview of the chemical versus physical etching contribution, we considered the gas chemistry of Cl_2 and N_2 involved in the plasma. Cl_2 is a reactive gas promoting the chemical etching of GaAs to form the following volatile species: $GaCl_x$ and $AsCl_x$. N_2 is a neutral gas promoting physical etching by ion bombardment. The SEM images in the tilted view (Figure 2a) show the GaAs etch rate and the angle between the nanostructure sidewall with a Si (100) bulk surface as a function of the Cl_2/N_2 gas ratio in the ICP with specific conditions (200 W), highlighting the resulting nanowire shape. The N_2 flow rate was fixed at 10 sccm, while the Cl_2 flow rate was varied from 10 to 80 sccm. The other process parameters were set constant: radio frequency power, 60 W; ICP power, 200 W; chamber pressure, 6 mTorr; and sample holder temperature, 35 °C. Optical emission spectrometry measurements, presented in Supporting Information Figure S1, show the Cl^{2+} quantities in the plasma. As expected, when the Cl_2/N_2 gas ratio was decreased, the reactive species quantity was reduced, and the plasma was highly physical. As the GaAs etch rate decreased, the etching selectivity between the HSQ mask and GaAs was very poor, leading to fast etching of the mask and preventing fabrication of high-aspect-ratio vertical nanowires (Figure 2a, left). Increasing the Cl_2 flow rate also increased the quantities of the reactive species as well as species renewal in the reactor. Thus, increasing the Cl_2 flow rate favored the chemical reaction over physical etching (ionic bombardment). As a consequence, the GaAs etch rate increased together with a

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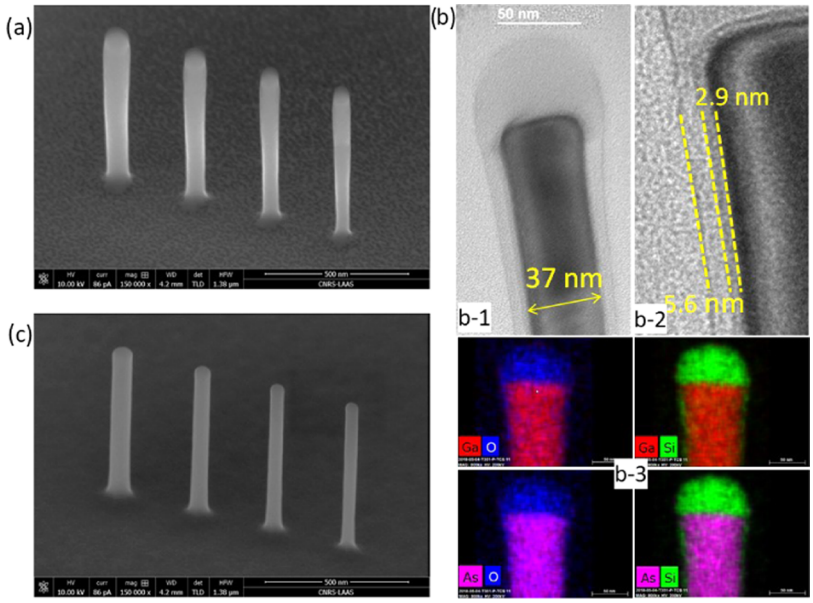


Figure 3. Characterization of the protective layer: SEM images in a tilted view (a) before and (c) after HF cleaning of GaAs vertical nanowires. (b) EDX-TEM *ex situ* analysis of the amorphous protective layer generated during the plasma etching step, which covers the GaAs vertical nanowires.

better HSQ selectivity, providing a very good improvement of the sidewall verticality (Figure 2a, right).

Next, to investigate the impact of the ICP coil power, the other process parameters were set constant: radio frequency power, 60 W; chamber pressure, 6 mTorr; Cl_2/N_2 gas ratio, 8; and holder temperature, 35 °C. Figure 2b shows the influence of the coil power on the GaAs etch rate and the verticality of the nanowire sidewalls, again with some specific conditions observed by SEM images in the tilted view. The ICP coil power controls the dissociation of the plasma in the reactive species and ions as well as the directionality of these particles. The increase of ICP power, from 0 to 500 W, increased the etch rate from 0.5 to 1.1 μm/min, thanks to a higher reactive species density that also had an impact on the sidewall verticality of the nanostructures.

When the ICP power remained low, the dissociation energy in the plasma was weak, generating a low quantity of Cl_2^+ and N_2^+ ions, as confirmed by optical emission spectrometry measurements at 1 and 50 W (see Supporting Information Figure S1). Moreover, N_2 has a bond-dissociation energy (BDE = 9.79 eV) much lower than that of Cl_2 (BDE = 2.51 eV). Therefore, the chemical reaction between Cl_2 and GaAs was favored over ionic bombardment. As chemical etching is mostly isotropic, the sidewall profile of the nanostructures has a "re-entering" shape, forming an angle with the Si(100) bulk surface lower than 90°. It was necessary to apply a sufficient power level to obtain a good balance between chemical and physical etching to tend toward a vertical profile (etching angle = 90°), which was reached with an ICP power of 200 W. If the ICP power was too high, the ion density would be very large, and the mean free path of ions would become very short, leading to more ion collision and ion deviation in the vertical direction. This configuration was more sensitive to a charge effect due to the HSQ dielectric mask, which could locally enhance the ion deviation. As shown in the SEM image in Figure 2b, a narrow part of the nanowire was overetched in the vicinity of the HSQ mask with an ICP power of 500 W. Finally, the optimal conditions to feature vertical GaAs nanowires were as follows: P_{ICP} = 200 W; P_{bias} = 60 W; Cl_2/N_2 = 8; P = 6 mT; and T = 35 °C.

Protective Layer. Figure 3a presents the SEM image in a tilted view after the plasma etching step using these optimized conditions. It shows that the top part is thicker than the bottom. In fact, it is expected that a covering layer forms during the chemical reaction and/or the redeposition of volatile compounds produced during the etching. The top part of the nanowire was thicker than the bottom part due to a cumulative effect during the etching.

Similar passivation has been observed previously on nanowire sidewalls during the etching of other III−V materials[29,30] using Cl_2/N_2 ICP reactive-ion etching. We, therefore, analyzed the NWs just after RIE by TEM. Figure 3b-1 presents *ex situ* EDX-TEM analysis of the nanowires performed on a TEM lamella lifted out using a focused ion beam (FIB) from the original substrate. This analysis confirms that an amorphous layer is present on the top and around the crystalline NWs. A high magnification image (Figure 3b-2) indicates that the amorphous layer formed on the nanowire sidewalls had a maximum thickness of approximately 9 nm on the top of the nanowire. This layer was composed of two sublayers: an inner layer (around 3 nm) and an outer layer (6 nm). The EDX maps, presented in Figure 3b-3, show that the outer amorphous layer was mainly composed of Si and O. Lateral concentration profiles extracted from the maps (not shown) clearly indicate that the Si/O layer is about 10 nm wide, in agreement with the TEM observation. In addition, the Ga profiles extend into the Si/O layer by around 2 nm more than the As one. Overall, these analyses show that the inner layer, around 3 nm thick, was a native oxide, probably Ga_2O_3 because Ga is preferentially oxidized over As. This inner layer extended under the HSQ mask. Interestingly, the outer layer, around 5.5 nm, did not contain any N element, indicating that a nonvolatile GaN or AsN complex was not formed on the sidewalls. These elements could be provided by the HSQ mask or from the Si carrier where the GaAs sample was stuck. Thanks to the good selectivity between SiO_2 and GaAs (1:6) with our optimized Cl_2/N_2 process conditions, the SiO_x

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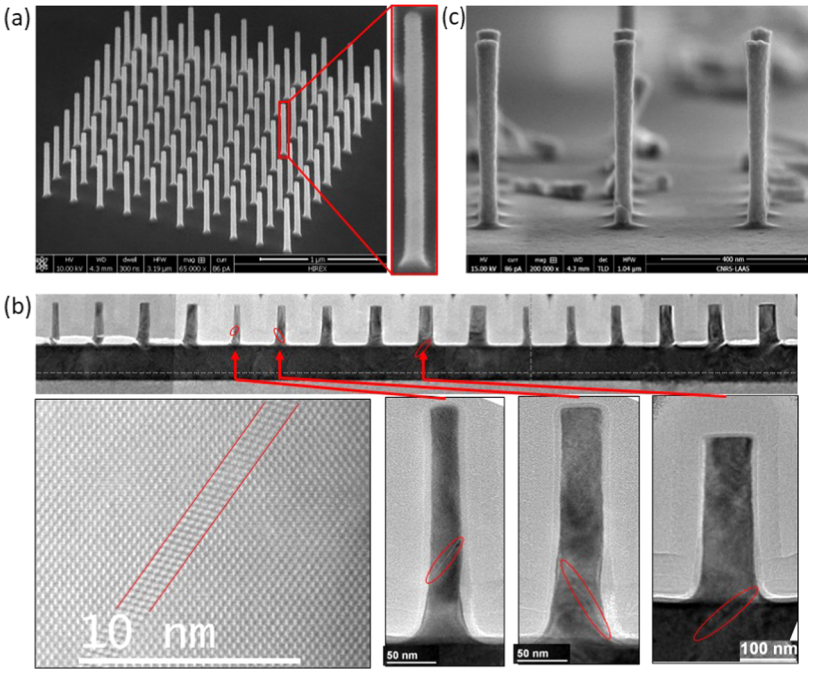


Figure 4. Nanowires with a high aspect ratio and structural characterization. (a) GaAs nanowire array on Si(100) with an aspect ratio up to 15 (diameter = 35 nm, height = 540 nm, pitch = 200 nm). (b) TEM observation of a FIB cross section on several GaAs nanowires showing the probability of defects with a nanowire. (c) GaSb nanowires (diameter = 50 nm, height = 660 nm, pitch = 400 nm) on a Si(100) wafer obtained following the same top-down strategy shown with patterned GaAs nanowires.

protective layer played an important role in obtaining the vertical sidewall by preventing isotropic chemical etching on the top part of the nanostructures.

Finally, Figure 3c shows the NWs after the wet chemical etch (1 min in 5% HF). The HF solution removes the covering layer. This SEM image (Figure 3c) shows perfectly homogeneous NWs. Therefore, the oxide layer was removed during HSQ mask stripping by HF.

Crystalline Defects and a Versatile Approach. Figure 4a shows the SEM image in a tilted view of an array of 100 GaAs nanowires with a pitch of 200 nm on Si(100) obtained using the optimized parameters presented below. The zoomed image of a nanowire highlights the very good diameter homogeneity (~35 nm) along its entire length (540 nm) and a high aspect ratio of 15. This demonstration of GaAs nanowires on a Si (100) substrate meets, for the first time, the requirements for nanowire device fabrication in terms of the control of localization, verticality, diameter, aspect ratio, and density. In addition, the roughness of the sidewall was very low, with an atomically flat interface demonstrated by high-angle annular dark-field scanning transmission electron microscopy analysis (not shown). Figure 4b presents the TEM cross-sectional analysis of 16 GaAs nanowires with different diameters. More than 80% of the nanowires exhibited defect-free crystalline structures. Crystalline defects could be observed on three nanowires. These defects were disoriented crystalline plans called "twinned planes" and were very localized in a defined region of the nanostructures without extension in the entire height. The impact of these defects on the electrical characteristics remains low compared to antiphase boundary defects. Indeed, the mobility and the resistivity have been measured on similar GaAs/Si substrates grown by metalorganic chemical vapor deposition with and without an antiphase boundary.[23] With antiphase boundary defects, the mobility was 10 times lower and the resistivity was 5 times higher compared to the GaAs layer used in the current study. In addition, the roughness of the sidewall was very low, with an atomically flat interface demonstrated by high-angle annular dark-field scanning transmission electron microscopy analysis.

Low-crystalline-defect epitaxial layer growth by metalorganic chemical vapor deposition on Si(100) can be extended to other materials.[25,39,40] In this study, the top-down structure approach, based on Cl_2/N_2 plasma etching, was applied with the optimized conditions on a GaSb layer. Figure 4c shows vertical GaSb nanowires on a Si(100) substrate with a length of 660 nm and a diameter of 50 nm, demonstrating the versatility of the approach and envisioning a possible cointegration of GaAs and GaSb vertical nanowires on the same standard Si(100) microelectronic substrate.

Axial Heterostructure GaAs/Si Nanowires. To add to the complexity of this work, we investigated the possibility of creating a GaAs/Si nanowire heterostructure based on the proposed top-down approach (Figure 5). The synthesis of heterostructured nanowires (axial[2] and core−shell[4]) is well known using the bottom-up approach[41,42] but it is much more difficult to address by the top-down approach.

Figure 5a schematically presents the process steps to fabricate axial heterostructured nanowires. First, the GaAs nanowires were patterned by etching the GaAs layer down to the Si/GaAs interface. After this step, 50 nm of the HSQ resist remained on top of the GaAs nanowires. At this stage, the Si etching step had to be selective with HSQ and not laterally etch the GaAs nanowires. For that, we have to choose plasma chemistry that protects sidewalls, as schematized by a green covering layer in Figure 5a. The false-color SEM image (Figure 5b) shows the result after the anisotropic Cl_2 plasma step usually used to define vertical Si nanostructures.[43] Pure Cl_2

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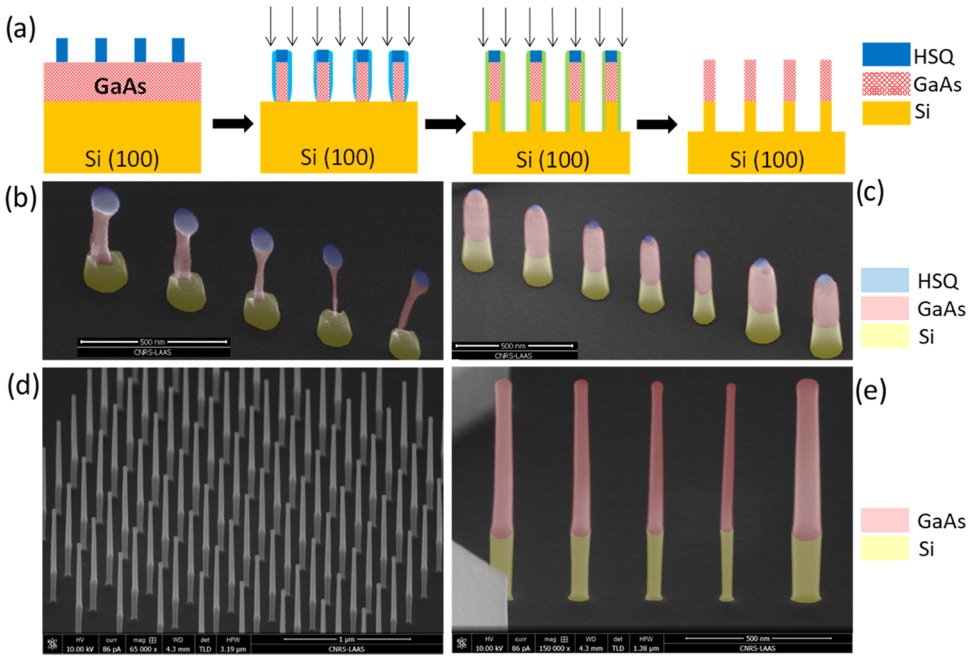


Figure 5. Heterostructured GaAs/Si nanowires: (a) Process flow chart. (b) Two successive plasma etchings (GaAs with the current plasma procedure followed by Si etching using plasma-based Cl_2 chemistry). (c) O_2 is added with Cl_2 to avoid anisotropic etching of the GaAs nanowires. (d) Two successive plasma etchings: Cl_2/N_2 plasma for GaAs nanowires and then $SF_6/C_4F_8/O_2$ plasma for Si nanowires, resulting in heterostructured GaAs/Si nanowires with a GaAs length of 640 nm and a Si length of 270 nm. (e) Colorized SEM image of 910 nm high heterostructured GaAs/Si nanowires with a diameter ranging between 40 and 90 nm.

plasma is highly isotropic due to GaAs nanowire degradation. To enhance the SiO_x layer deposition and to protect the GaAs nanowire sidewall, short O_2 plasma cycles were added during the Cl_2 etching process (O_2 plasma for 30 s and Cl_2 plasma for 30 s), and GaAs/Si nanowires with an axial heterostructure were obtained (Figure 5b). However, the main drawback of these cycles of Cl_2 plasma/O_2 plasma was the poor selectivity between HSQ and Si (~1). To improve this situation, a process based on fluorine chemistry ($SF_6/C_4F_8/O_2$) was introduced, providing a Si/HSQ selectivity of 5. Figure 5d shows the SEM images of a network of 100 heterostructured GaAs/Si nanowires with a diameter of 40 nm and a pitch between nanowires of 200 nm. The colorized SEM image shown in Figure 5e demonstrates 910 nm high heterostructured GaAs/Si nanowires with a diameter ranging between 40 and 90 nm. For perfect patterning of these heterostructured nanowires, the challenge is to master the transition between the two etching chemistries without degrading the Si/GaAs interface. Therefore, detection of the endpoint during GaAs etching is critical. This Si/GaAs interface is detailed in Supporting Information Figure S2. The overetching of GaAs must be less than 3 s; otherwise, the lateral etching at the bottom of the nanowires would be accentuated, resulting in mechanical fragility of the nanowires and carrier mobility scattering.

CONCLUSIONS

For the first time, we demonstrated the fabrication of a vertical III−V (GaAs or GaSb) nanowire array on a standard Si(100) microelectronic platform by a wafer-scale approach that is complementary metal−oxide−semiconductor compatible using low-corrosive chlorine-based chemistry. III−V nanowires patterned on a Si(100) substrate with a high aspect ratio (up to 15). The nanostructures were structurally characterized to evaluate the crystalline defects of the GaAs nanowires. This top-down approach enables perfect control of all of the nanostructure features (location, verticality, diameter, aspect ratio, and density). Moreover, this approach was pushed forward by combining two sequential plasma etching steps to pattern GaAs−Si nanowires with an axial heterostructure that has a diameter of 40 nm and a length of 900 nm. This large-scale technology on the Si(100) platform paves the way for new integration schemes for large-scale applications in nanoelectronics, nanophotonics, or photovoltaics.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.1c05876.

Figure S.1: Optical emission spectrometry (OES) measurements OES at 1 and 50 W and Figure S.2: endpoint detection during GaAs etching to master the GaAs/Si interface of heterostructured nanowires (PDF).

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Notes

The authors declare no competing financial interest.

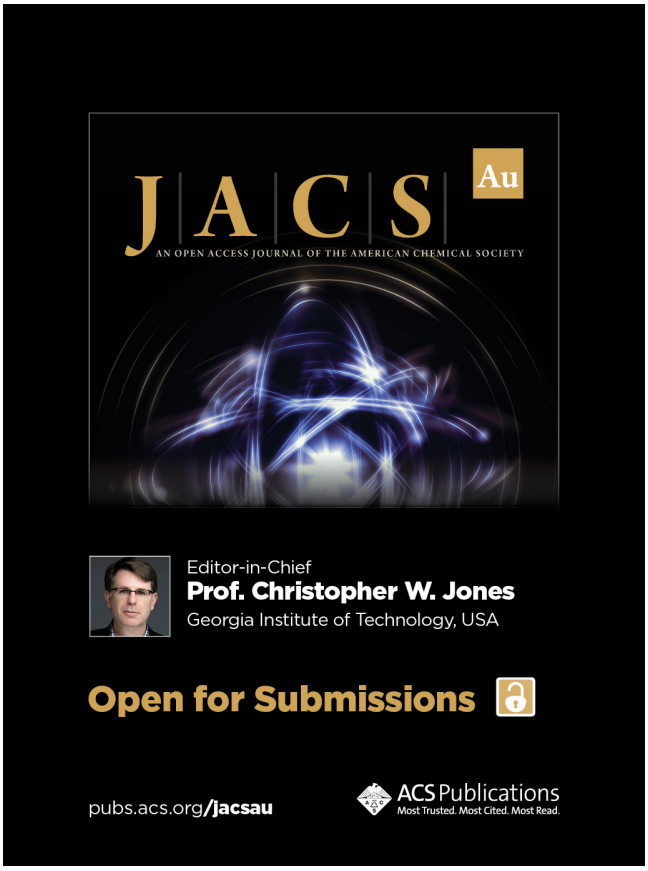
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