A Technique to Assess Conducted Immunity of an Electronic Equipment after an Obsolete Integrated Circuit Change

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***Abstract*—This paper describes a fast methodology for managing the obsolescence issues of integrated circuits in industrial equipment (aeronautical or automotive). The objective is to predict EMC non-compliance risk, especially for conducted immunity, after a component change. Based on black box modeling using S-parameters, this experimental approach consists in declining the conducted immunity requirements, from the input of the equipment to the pins of the replaced component. Once this transfer function is established, a link is envisaged between the immunity level determined at the boundary of the component to be replaced and that of the new one. This link allows the prediction of EMC non-compliance risk level, from an equivalent test at the component level, due to a change of a component.**

Keywords—Obsolescence, Integrated circuit, Conducted immunity, Direct Power Injection.

I. Introduction

A simple comparison of the commercial lifetime of electronic components (approximately 3 to 5 years) and that of electronic equipment and systems (15 to 40 years for an aircraft, for example) shows the inevitable problem of rapid obsolescence of integrated circuits (IC). To remain compliant with standards, any change of an obsolete component must lead the Original Equipment Manufacturers (OEM) to requalify their products to prove the non-regression of their EMC performances. The requalification usually requires time-consuming tests, significant costs and delays. Currently, the standard EMC measurement method is the only authorized method to validate EMC of an equipment.

Different approaches have been deployed for managing consequences of electronic component obsolescence on EMC. A common approach to avoid requalification proposes a complete and exact modeling of the equipment according to a bottom-up vision. It relies on the development of models at the component, board and equipment levels [1] [2] [3] [4]. They are usually based on electromagnetic 3D modeling and full-wave simulations [5]. However, these approaches quickly find their limits due to the complexity of electronic equipment and the long modeling time. In addition, the exact information regarding each part of the equipment is not necessarily known for confidentiality reasons. These drawbacks severely limit the use of these methods and could be, in some cases, not envisaged due to the cost and delays.

In many cases, a complete requalification of the equipment is not essential to assess a risk of non-compliance, especially if the change concerns only one IC and introduces no modification of the equipment design. It could be advantageous to assess the impact of the change of this IC on the EMC performances of the equipment, by testing only the EMC of the IC, since EMC of IC tests remain cheaper than equipment-level tests. This is the aim of this paper, which proposes an approach based on EMC measurements at component level to estimate the non-regression of equipment in the context of the component obsolescence. Here, only conducted immunity (CI) along cable harness is considered, such as in Bulk Current Injection (BCI) test as defined by ISO11452-4 or RTCA/DO-160 standards. The proposed approach aims to decline the CI defined at the equipment input into a disturbance level defined at the boundary of the replacement IC, i.e. the component used to replace the obsolete IC. The residual level of disturbance that reaches the IC pins can be determined by S-parameter measurements made at the equipment input connector, according to the methodology presented in [6]. The EMC risk assessment could be achieved by a conducted immunity test directly done at IC level, for example by the Direct Power Injection (DPI) method [7].

The paper is organized as follows: the approach is described in Section II. A validation case study, based on an op-amp dedicated to current measurement through a shunt resistor, is proposed and presented in Section III. The proposed approach relies on an equivalent model of the equipment and the DPI test-bench. Details about the modeling process are provided in Section IV. Section V illustrates the proposed methodology through the analysis of results on the case study.

II. Presentation of the Approach

A. General Assumptions

The studied equipment is assumed reciprocal and linear. The non-linear behavior of the components (e.g. active circuits, protection structures, etc.) is neglected. The general ground of the system, which is usually mounted within a shielded enclosure, could be different from the local component ground (usually a local ground plane at PCB level). In this study, only conducted injection on the harness is considered and is common-mode type. The disturbance

induced by the injection system and driving on the harness is modeled as an equivalent Thévenin generator placed at the input connector of the equipment. The method to determine this equivalent source in BCI test is not covered in this paper. Interested readers could find information about this topic in papers such as [8] [9] [10] [11].

B. General approach

The purpose of the approach is to decline the normative constraint from the input of equipment to the input of the replacement component such as the common or differential voltage applied to the pins of the component to change. An equivalence between CI tests at equipment and IC levels has to be found, such as illustrated in Fig. 1. An important assumption has to be made: the same failure mechanism arises during both CI tests, with the same amount of residual disturbance V_{IC} applied on IC pins.

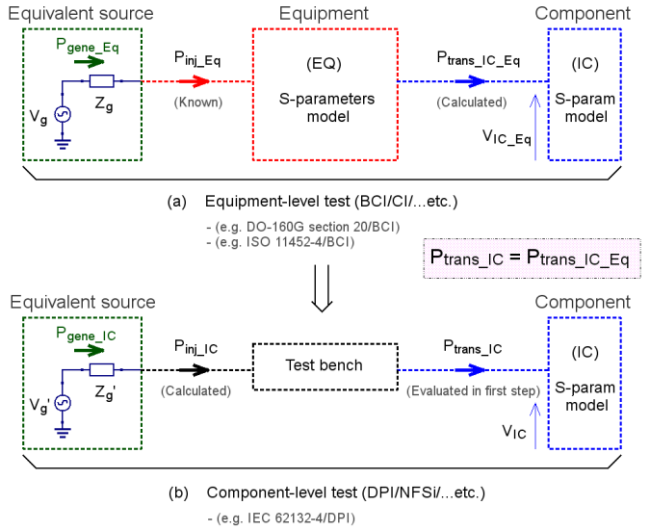

Fig. 1. Equivalence between conducted immunty test at equipment and component level

In Fig. 1-a, the equivalent model of CI test at equipment level is illustrated. The injection source, the coupling device and the cable harness are modeled by an equivalent Thévenin generator. If the transfer function of the equipment (i.e. all the interconnects and devices between the equipment input connector and the replacement IC) is known, the amplitude of the equivalent Thévenin generator V_g required to induce V_{IC} at the IC pin can be determined. In this paper, the disturbance amplitude provided by the generator in equipment and IC tests is defined in terms of available power, as given by (1). In the equipment test, the power provided by the equivalent disturbance source V_g to the equipment input is noted P_{inj_Eq} and is given by (2). It represents the amount of disturbance that the equipment has to fulfill.

$$P_{gene} = P_{max\_available} = {V_g}^2 \Big/ 4\,Z_g \tag{1}$$

$$P_{inj\_Eq\,(W)} = P_{gene\_Eq}\ (1 - |\Gamma_{in\_Eq}|^2) \tag{2}$$

where Γ_{in_Eq} is the reflection coefficient seen at the equipment input and is given by (3) for a two-port equipment characterized by its S parameters. Γ_{IC} is the reflection coefficient at the replacement IC input. Similarly, Fig. 1-b shows the equivalent model of the CI test at IC level. If the transfer function of the CI test bench is known, the power P_{inj_IC} provided by the disturbance source required to induce V_{IC} at the IC pin can also be determined according to (4).

$$\Gamma_{in\_Eq} = S_{11Eq} + \frac{S_{12Eq}S_{21Eq}\Gamma_{IC}}{1-S_{22Eq}\Gamma_{IC}} \tag{3}$$

$$P_{inj\_IC} = P_{trans\_IC}\,\frac{(1-|\Gamma_{inDPI}|^2)\,|1-S_{22DPI}\Gamma_{IC}|^2}{|S_{21DPI}|^2\,(1-|\Gamma_{IC}|^2)} \tag{4}$$

Where Γ_{inDPI} is the reflection coefficient seen at the input of the DPI test bench. It is computed as (3) for a two-port equipment characterized by its S parameters. P_{trans_IC} is the power transmitted to the IC and is given by (5), where Z_{IC} is the input impedance of the replacement IC.

$$P_{trans\_IC} = \frac{|V_{IC}|^2}{Z_{IC}} \tag{5}$$

Thus, an equivalence between the disturbance sources in CI tests at equipment and IC levels can be found to induce the same effect on the considered IC. In other words, if the immunity level of the equipment is defined in terms of a power P_{inj_Eq}, this level can be translated into an equivalent power P_{inj_IC} during the IC immunity test. If P_{inj_IC} is applied during the IC test and if the IC is still operational, this IC should be still operational during the equipment test when P_{inj_Eq} is applied. For this demonstration, we used the DPI method as the immunity test because it is well suited for the conducted immunity. Also, for its simplicity in terms of test set-up and analysis, it is easy to measure the power and to calculate the voltage and the current at the IC level compared to other immunity tests (e.g. TEM cell or NFSi tests). The repeatability of DPI measurements is good. Furthermore, this test is widely used by most component manufacturers.

C. Detailed description

The different steps of the EMC risk assessment methodology are described in Fig. 2. In the following part, IC stands for the replacement IC. In a typical situation, an immunity level is defined at equipment level (e.g. the maximum amount of current induced in the equipment cable harness in a BCI test). The first step, not covered in this paper, consists in translating this immunity level into the available power of an equivalent disturbance source. In this study, the immunity level defined at equipment level is assumed the amount of power that the equipment has to fulfill (P_{inj_Eq}).

According to Fig. 1, the initial step is to create the equivalent black box model of the equipment and IC. This model is built from two measurements: the first one, described in Section IV, concerns the extraction of the equipment transfer function, which describes the filtering provided by connectors, interconnects and devices mounted between the connector input and IC. The second one aims at measuring the input impedance seen from the input IC pin (in terms of S-parameters). The next step consists in calculating the power P_{gene_Eq}, using (2), from P_{inj_Eq} and the parameter Γ_{in_Eq}. Then, converting this power to an equivalent Thévenin generator, using (1), where $Z_g = 50\ \Omega$. Therefore, the voltage V_{IC_Eq} applied on IC during the equipment immunity test can be easily extracted by simulation, the current as well. The power $P_{trans\_IC\_Eq}$ can be calculated by (5).

The same failure mechanism occurs during an IC test with the same residual disturbance ($V_{IC} = V_{IC\_Eq}$) and with the

same power that causes the failure ($P_{trans\_IC\_Eq} = P_{trans\_IC}$). Consequently, the DPI test level P_{inj_IC} equivalent to the equipment test is computed from an equivalent model of the DPI test bench and the IC. Black-box modeling based on S-parameter measurements can be done on the different elements of the DPI test bench to accelerate the modeling process. Once P_{inj_IC} has been determined, the setpoint DPI power P_{gene_IC} can be calculated and the equivalent Thévenin generator that provides P_{inj_IC} can be determined as explained previously. P_{gene_IC} will be the reference of the evaluation of the replacement IC. DPI test can therefore be performed on IC and the EMC risk due to the IC change can be evaluated. This procedure requires only the development of a specific test board for the DPI test. If a generic test board dedicated to common IC package is developed, this board can be reused so that the overall cost of this procedure can be reduced.

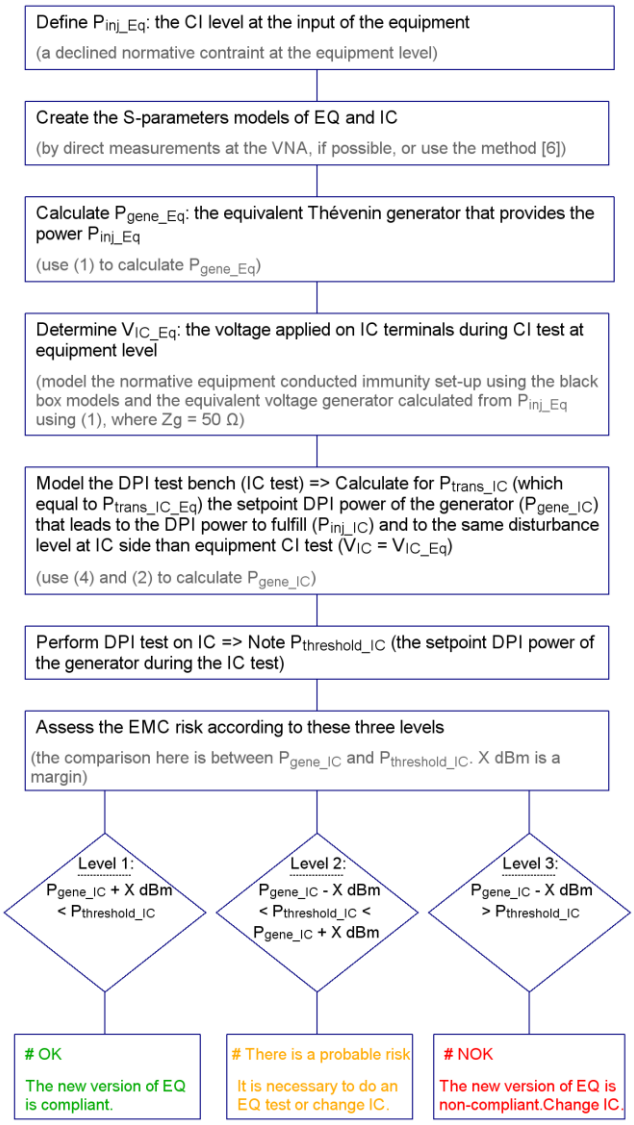

Fig. 2. Flowchart of the EMC risk assessment methodology

The risk assessment is based on a comparison between the DPI test results $P_{threshold\_IC}$, that represents the setpoint power of the generator during the test made on IC, and the limit P_{gene_IC}. An error margin has to be accounted for in order to compensate the uncertainties related to equipment transfer function and DPI test bench measurement errors. Measurement test bench can be extracted from an uncertainty budget applied on the DPI test bench, for example based on standard method such as CISPR 16-4-2 [12]. An additional safety margin may also be introduced by the OEM. In this study, from several repeated measurements, the DPI test bench repeatability is evaluated to 1 dB and an arbitrary additional margin of 2 dB is introduced, so that the error margin is set to 3 dB.

The risk assessment is done according to the following methodology: the susceptibility level $P_{threshold\_IC}$ of the IC is determined at each test frequency. Then, it is compared to P_{gene_IC}. The risk assessment is done according to the strategy of the three levels described in Fig. 2. If the IC fails for DPI power larger than P_{gene_IC} plus the error margin, the introduction of the IC in the equipment will not compromise its immunity and the equipment CI requalification is not necessary. Moreover, the gain in terms of EMC margin provided by the IC can be computed. In contrary, if the IC fails for DPI power less than P_{gene_IC} minus the error margin, the immunity of the equipment will regress with this new IC and a CI requalification of the equipment is not necessary. The requalification becomes necessary if the IC fails for DPI power comprised between P_{gene_IC} plus or minus the error margin.

III. Presentation of the Case Study

A. Tested Circuit

The tested circuit is an operational amplifier, AD8515 from Analog Devices, mounted in a non-inverter configuration for a current sense application based on a shunt resistor, further information on this application are available in [13]. The electrical diagram of the tested application is presented in Fig. 3. The circuit is powered by a 5 V DC voltage source. In this study, the disturbance is applied on the power supply and leads to the generation of offset on the amplifier output voltage V_{OUT}. When the offset voltage exceeds 5 mV, a failure is detected. The differential amplifier is mounted on a daughter 4-layer board, which is also connected to a mother board (Fig. 4). For the sake of the validation of the proposed approach, the differential amplifier is considered as the IC to be replaced. The SMA connector *Vcc* is the IC input. The new IC version consists in the introduction of a RC filter at the non-inverter input, as shown in Fig. 3. In the following part, the initial IC version is noted IC1 while the new version is called IC2. The mother board is supposed to be the equipment. It contains two microstrip lines routed on a FR4 substrate 4-layers PCB connected to SMA connectors.

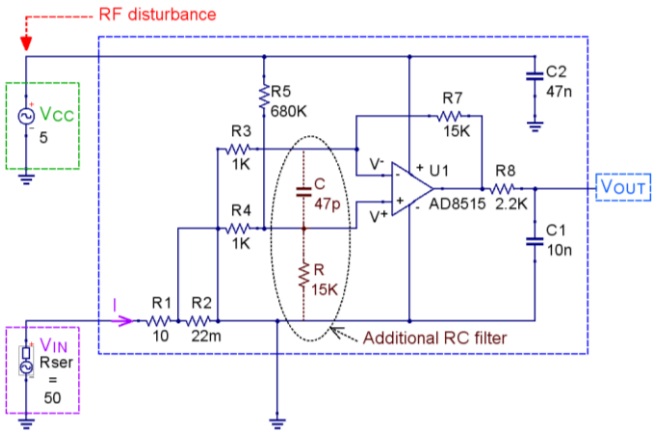

Fig. 3. Schematic of the tested application (IC1 board, IC2 board: IC1 board + additional RC filter)

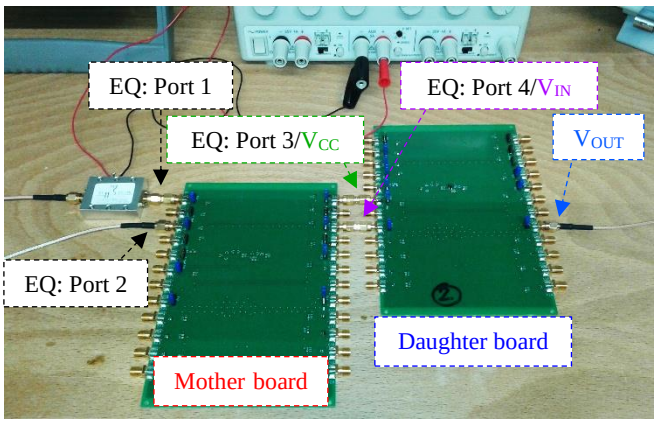

Fig. 4. Equipment under test: mother board (left) and daughter board (right)

B. DPI Test Bench

The DPI test bench is illustrated in Fig. 5. It consists of an RF synthesizer (Rohde & Schwarz SMB 100A; 9 kHz–3.2 GHz), a 30 W RF power amplifier (BONN Elektronik BSA 1001-30D; 100 kHz–1 GHz), a bidirectional internal coupler and RF power meter (Rohde & Schwarz NRP-Z91) to monitor the forward power. The RF disturbance is superimposed to the 5 V power supply through a bias tee (10 MHz–6 GHz) available off-the-shelf from several vendors. The bias-tee output is connected to the *Vcc* of the daughter board through an SMA connector. The input (V_{IN}) of this board is connected directly to a waveform generator (Keysight 33500B Series) which generates a ramp signal (10 V peak to peak with a frequency of 400 MHz). The DPI test is performed with 51 points linearly spaced between 10 MHz and 1 GHz. The maximum amount of forward power is limited to 40 dBm.

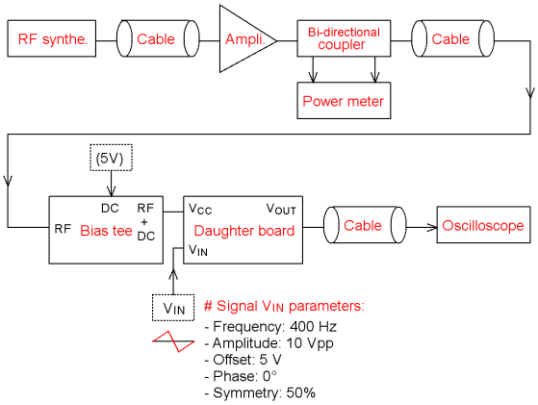

Fig. 5. Simplified schematic diagram of the DPI test bench

C. Equipment Conducted Immunity Test

A CI test is also realized at equipment level. The DPI test-bench is reused. The bias-tee output is connected to the port 1 of the mother board through an SMA connector as shown in Fig. 4.

IV. Modeling of the Equipment and the Test Bench

As described in Fig. 2, the proposed methodology to assess EMC risk is based on modeling of equipment CI immunity and DPI test benches. In order to ensure a fast modeling process, a black-box modeling approach based on S-parameter measurements is applied. As all the equipment of the CI test bench and the devices mounted on the equipment behave linearly, this approach remains valid. The simulations are performed with the freeware QUCS [14]. Fig. 7 describe the models of the equipment CI and DPI test benches. The S-parameters of the coupler, the bias tee, the cables, the equipment board and the IC input have been measured with a VNA and introduced in S-parameter boxes in QUCS.

In both models, the disturbance source takes into account the variable gain of the power amplifier. The QUCS component library does not include a variable voltage source that operates in frequency domain. We have created a simple model of an equivalent generator with variable gain. The voltage V_g is calculated from the power P_{gene} according to (1) where $Z_g = 50\ \Omega$. This variable voltage (integrated in a touchstone file) is represented as an impedance in parallel with a 1A current source. The output of this circuit is connected to voltage-controlled voltage source.

A critical part of the modeling process is related to the measurement of the transfer function of the equipment, defined between the input connector of the equipment and the input pin of the IC to change. This transfer function is required to determine the amplitude of the residual disturbance that reaches the IC pins. This measurement could be easily done if proper RF ports exist both at input connector and at IC side. However, the component terminals are usually not accessible to place an S-parameter measurement port. Nevertheless, if the IC can be removed and replaced by some passive loads, the transfer function can be determined by an indirect S-parameter measurement, made at the input connector side. The method, initially proposed in [15] and adapted to the case of IC change in [6], is used to extract the S-parameters matrix between the input and output ports of the equipment board, as a demonstrator, only from S-parameter measurements done at the input ports. Fig. 6 shows a comparison between some S-parameters measured directly and those extracted by the indirect method.

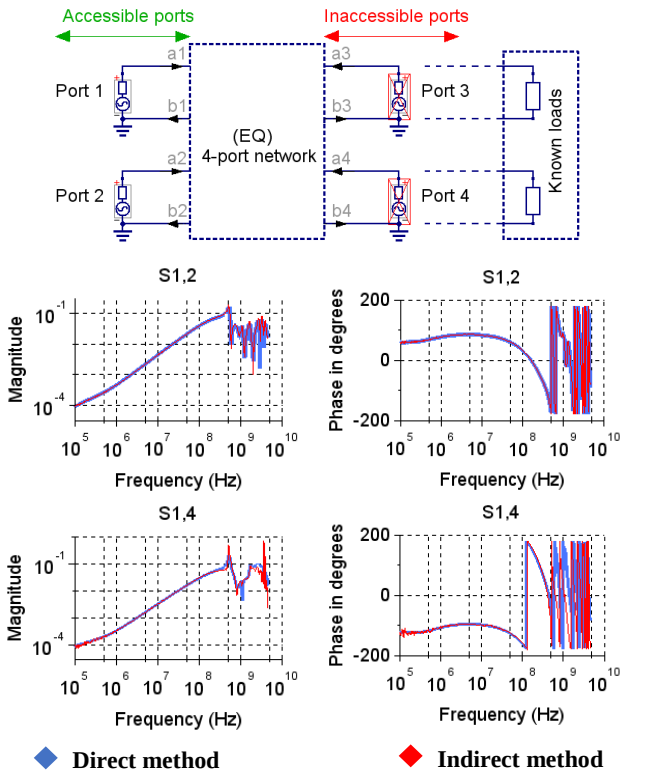

Fig. 6. Illustration of the indirect measurement method for S-parameters; example of some estimated S-parameters vs. fully measured S-parameters (Frequency: 100 kHz - 4.5 GHz)

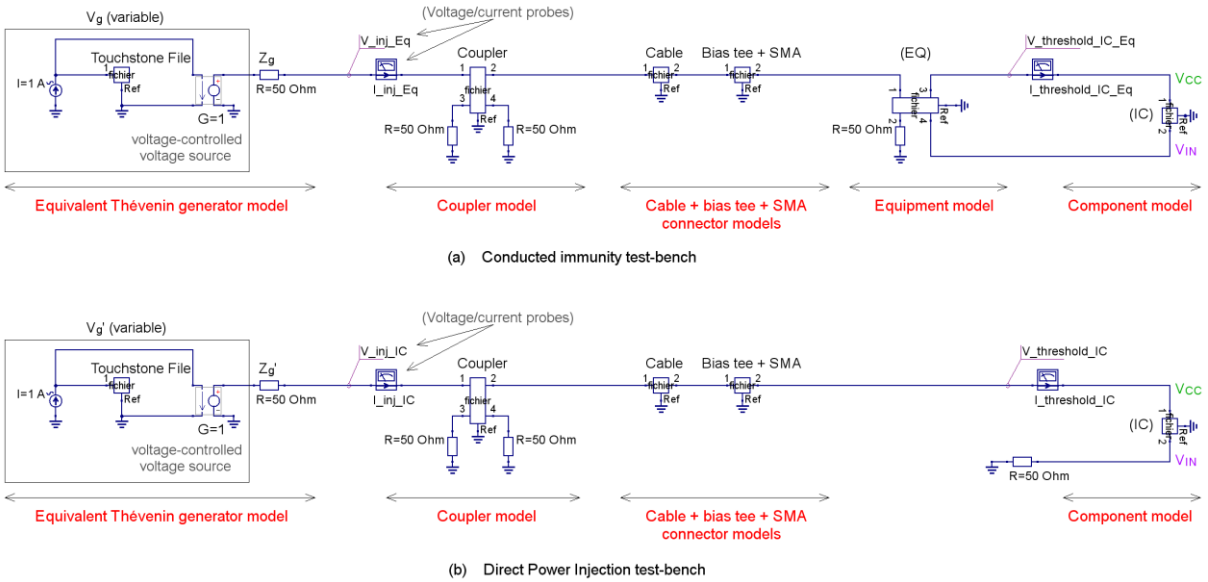

Fig. 7. Equivalent model of both conducted immunity and DPI test-bench

V. Validation of the Approach

A. Immunity of the components

Fig. 8 presents the susceptibility level of IC1 and IC2 during the DPI test. This result shows that both IC versions exhibit sufficiently different susceptibility levels that the proposed approach has to detect. Except between 386 and 426 MHz, the IC2 version is more immune than IC1. Note, due to forward power limitation, no default is detect for IC2 below 100 MHz.

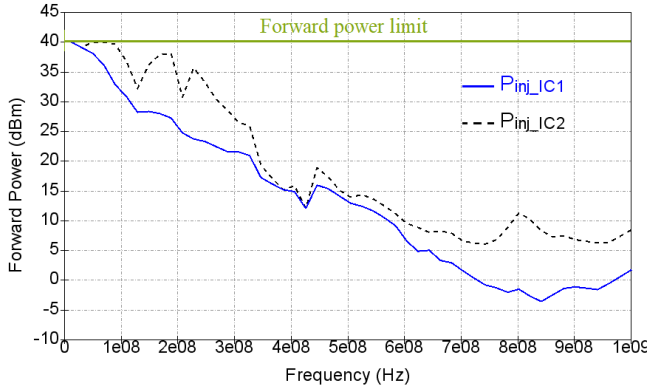

Fig. 8. Conducted immunity of IC1 and IC2 (forward power)

B. Voltage and current applied on the components

An initial analysis is done to verify the general assumption on which relies the proposed approach: the equivalence of voltage level applied on IC pin during the CI equipment and the DPI test. From the DPI and equipment CI test results done on both equipment versions and the models of both test benches, the voltage and current at the input of the IC are computed. Fig. 9 compares the voltage and current at IC pin during both tests, when IC2 is mounted. Voltage and currents determined during both tests are nearly identical. Some differences are visible between 10 and 100 MHz. Actually, no failures arise on this frequency range and the injection power reaches the power limit. There are also some differences around 400 MHz, which are certainly related to repeatability issue of the DPI test bench. This result confirms the hypothesis about the equivalence of applied voltage on IC pin during both immunity tests at equipment and IC level.

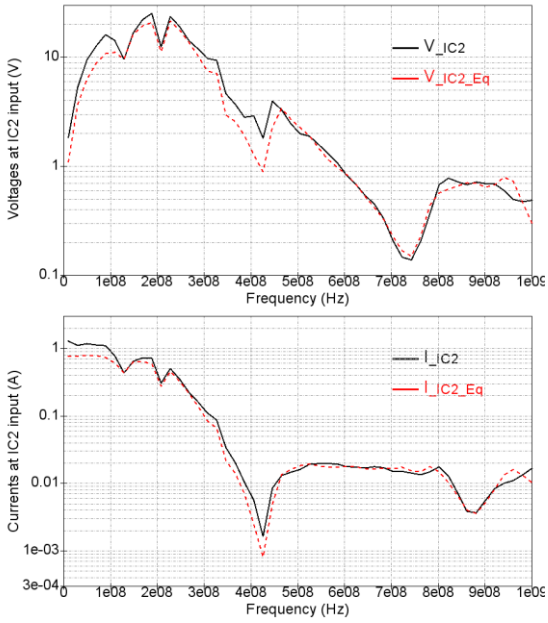

Fig. 9. Comparison of voltage (top) and current (bottom) at IC2 input during CI and DPI tests

C. Evaluation of the risk of EMC non-compliance

In this part, the risk assessment linked to a change of component is illustrated when IC2 replaces IC1. The purpose is to perform a DPI test on the "new" component IC2 to determine if no EMC risks are created by the introduction of this new component and if requalification test at equipment level is required. To this end, the methodology presented in Section II is used. The immunity target at equipment level P_{inj_Eq} is defined as the forward power measured during the CI test on the equipment with IC1. From the models of the CI test bench, the equipment and the input impedance of IC1, the power transmitted to IC1 is determined. Then, from the DPI test bench model, the setpoint DPI power P_{gene_IC1} to reach this voltage level during the DPI test is computed. This level, shown in Fig. 10 constitutes the power target that IC2 has to withstand during the DPI test.

An immunity test is done on IC2 to measure its susceptibility threshold and compare it to the power target determined from the equipment CI level on IC1, in its obsolete version which has already been established. Both results are compared in Fig. 10. Two limits located at +/- 3 dB around the power target curve are added to show the error margin. This result shows that the immunity threshold of IC2 is equal or larger than the power target, proving that the introduction of IC2 in the equipment should not reduce its immunity compared to the initial version. However, the EMC margin introduced by IC2 is less than the error margin between 350 and 640 MHz. The confidence in the lack of EMC regression is not sufficient, so that a CI requalification of the equipment should be considered, in particular is this frequency range.

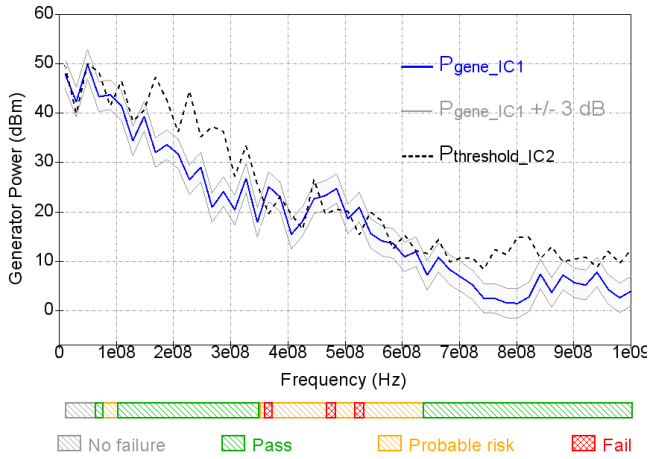

Fig. 10. Comparaison between the measured generator power of the DPI test on IC2 and that calculated from the equipment conducted immunity test (top) - EMC risk assessment (bottom)

VI. Conclusion - Perspectives

The paper has presented a method to assess the risk of regression of the conducted immunity of an electronic equipment due to the change of a circuit. Such a situation usually implies a complete requalification of the equipment with the replacement circuit. The approach described in this paper proposes to replace this costly test by a DPI test performed only on the replacement circuit in order to determine if:

- The requalification test can be omitted since the replacement circuit introduces a sufficient EMC margin.
- The requalification test can be omitted because the replacement circuit is significantly more susceptible than the original one and an alternative solution should be identified.
- The requalification test is necessary on the frequency ranges where the EMC margin is not sufficient.

It is important to note that this approach allows estimating the real margin of a normative test from the DPI test on the component. Information that could really help the manufacturers in the specification of margins.

This approach requires the development of two equivalent models about the equipment and the DPI test bench. Both models can be built from S-parameter measurements in order to limit the cost of the modeling process. The only extra cost of this approach is related to the development of a test board for the DPI test of the replacement circuit. Two issues are not addressed in this paper. The first concerns the modeling of the CI test bench in an equivalent disturbance source and the estimation of the error margins due to measurement errors. The second concerns the uncertainties of the equipment transfer function. Further studies are required to address these issues and confirm the validity of the approach on a component change scenario.

Acknowledgment

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