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# Sub-10-nm Diameter GaSb/InAs Vertical Nanowire Esaki Diodes with Ideal Scaling Behavior: Experiments and Simulations

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**Abstract**—We present the first experimental demonstration of sub-10-nm diameter GaSb/InAs vertical nanowire (VNW) Esaki diodes. Our devices exhibit excellent current scaling behavior over nearly two decades of diameter. An average Esaki peak current density of 1 MA/cm<sup>2</sup> is obtained, among the best when projecting from the state-of-the-art at our nominal doping level. An average current density of 4 MA/cm<sup>2</sup> is demonstrated at  $V_{ds} = 0.3$  V, which is promising for future ultra-low power VNW tunnel FET applications based on this material system. NEGF quantum transport simulations are carried out. Inelastic tunneling due to phonon emission is found to suppress tunneling current in the positive  $V_{ds}$  branch and to widen the Esaki peak in the negative  $V_{ds}$  branch, which has long been underestimated.

## I. INTRODUCTION

In an effort to reduce transistor power consumption in logic applications, Tunnel FETs (TFETs), which exploit band-to-band tunneling (BTBT), have attracted great interest [1]. Experimental demonstrations to date have suffered from low drive current, which severely limits logic performance. Among all possible designs, the GaSb/InAs system offers the greatest potential [2] thanks to its broken-band alignment and the excellent transport properties of III-V materials [3]. Composition/doping abruptness and interface trap density are of key importance to the GaSb/InAs tunneling junction, the core of the TFET. To date, highly-scaled GaSb/InAs TFETs have only been demonstrated through bottom-up approaches using MOVPE [4]. This yields limited junction sharpness, and thus low BTBT current, as compared with MBE.

In this work, in order to assess the ultimate TFET potential of the GaSb/InAs system, we have fabricated sub-10-nm vertical nanowire (VNW) Esaki diodes on an MBE-grown heterostructure through a well-optimized top-down approach. Quantum transport simulations have been performed with the goal of understanding the limiting physics. Our results demonstrate the extraordinary prospects of GaSb/InAs TFETs for logic applications.

## II. PROCESS TECHNOLOGY

**Fig. 1** shows the starting heterostructure grown by MBE and the finished device cross-sectional view. GaSb substrate is chosen to minimize lattice mismatch within different layers. From bottom to top, a p<sup>++</sup>-GaSb layer with 1000 nm thickness is grown on an n-type GaSb substrate. This layer serves both as buffer layer and the source of the Esaki diode. A 15 nm n<sup>+</sup>-InAs layer is subsequently grown to form an abrupt tunneling junction. To make the layers fully strained, a 60 nm n<sup>+</sup>-InAs<sub>0.91</sub>Sb<sub>0.09</sub> layer lattice matched to GaSb is then grown. This is followed by a 15 nm n<sup>++</sup>-InAs layer to enable a good top ohmic contact. Since Si is a p-type dopant in GaSb but an n-type dopant in InAs, an abrupt doping profile is achieved by using Si as dopant across the junction.

The device fabrication process flow is described in **Fig. 2**. We leverage two key etching technologies from our previous studies, i.e., chlorine-based reactive ion etching (RIE) [5] and alcohol-based digital etch (DE) [6, 7]. **Fig. 3** shows a 24-nm-diameter VNW fabricated by RIE (left) and, subsequently, after 4 cycles of DE with a final diameter of  $D(\text{GaSb}) = 9$  nm, featuring a smooth sidewall. DE rate on GaSb is found to be ~2 times faster than that on InAs(Sb), due to the higher oxidation rate of GaSb in pure oxygen. Immediately after DE, 5 nm Al<sub>2</sub>O<sub>3</sub> is deposited by ALD for passivation. Spin-on-glass (SOG) is then applied to planarize VNWs, followed by CF<sub>4</sub> RIE to open drain and source contact vias. Al<sub>2</sub>O<sub>3</sub> is wet etched by TMAH and Ni/Mo is then sputtered for ohmic contact. Finally, Ti/Au probe pads are fabricated by lift-off.

The final devices feature a single VNW with  $D(\text{GaSb})$  ranging from 9 nm to 1000 nm. Two samples (samples 1 and 2) are fabricated at different times through an identical process except that more DE cycles are applied on the latter one.

## III. ELECTRICAL CHARACTERISTICS

In this paper, we use a TFET-like voltage sign convention ( $V_{ds}$ ) such that a positive  $V_{ds}$  refers to the reverse regime of the pn junction where the n-region is positive with respect to the p-region. All current density values are calculated with respect to the cross-sectional area of GaSb since that is the narrowest point of the tunneling junction.

**Fig. 4** shows I-V characteristics at room temperature (RT) of an exemplar  $D(\text{GaSb}) = 11$  nm device exhibiting clear Esaki diode behavior with a peak current density of 2.3 MA/cm<sup>2</sup> and a peak-to-valley current ratio (PVCR) of 2.1. Negligible hysteresis is observed. **Fig. 5** shows I-V characteristics of three different  $D(\text{GaSb}) = 9$  nm devices exhibiting clear negative differential resistance (NDR) characteristic of Esaki BTBT. A superlinear turn-on for positive  $V_{ds}$  indicates the existence of a small energy barrier most likely associated with the top contact due to the tiny contact area. This is only observed for sub-10-nm devices. Further improvement is needed to minimize contact resistance.

Temperature-dependent I-V measurements are carried out on devices with different diameters. For a  $D(\text{GaSb}) = 11$  nm device (**Fig. 6**, left), a nearly constant peak current density independent of T is found. PVCR increases from 2.6 at RT to 4.4 at 77 K, mainly due to the suppression of trap-assisted tunneling (TAT) at the Esaki valley [8]. For large negative  $V_{ds}$ , the thermally-activated current component from thermionic emission and electron-hole recombination is limited by series resistance. For positive  $V_{ds}$ , the current is temperature-independent, consistent with a dominant BTBT process. In a larger device (**Fig. 6**, right), the current is absolutely temperature-independent except for large negative  $V_{ds}$ . This indicates a high-quality tunneling junction with a small interface trap concentration.

**Fig. 7** shows I-V characteristics of devices with D(GaSb) ranging from 9 nm to 1000 nm. Typical PVCR is  $> 2$ , with a maximum of 3.5, close to the best in the literature [9]. The peak voltage (the absolute value of  $V_{ds}$  at which the peak current occurs) is independent of current level except for the smallest and the largest devices, which both suffer from series resistance. For the smallest device, the excess resistance is due to a non-optimal top contact. For the largest device, it is due to non-scalable resistance of probe pads and probe tips [10], which is estimated to be  $\sim 30 \Omega$  in our devices.

To study the diameter scaling behavior, peak current and peak current density vs. D(GaSb) are plotted in **Fig. 8**. For all devices exhibiting NDR, a quadratic relationship between peak current and GaSb diameter is demonstrated (left) over the entire two decades of diameter range. The average peak current density is  $1 \text{ MA/cm}^2$  (middle). Peak current scaling in both samples 1 and 2 is identical. This is in spite of the fact that passivated VNWs after RIE, DE and ALD from samples 1 and 2 (right) have a similar D(GaSb) = 9 and 10 nm, but quite different D(InAs) = 19 and 35 nm, respectively. The indistinguishable current density in both samples suggests that BTBT is primarily limited by the GaSb side of the junction.

The suitability of this material system and our process technology for ultra-low power VNW TFET applications can be assessed by examining the current density at  $V_{ds} = 0.3 \text{ V}$ , as shown in **Fig. 9**. The somehow more scattered data distribution as compared with the peak current (**Fig. 8**) is due to the greater impact of contact resistance. Ideal scaling is shown across most of the diameter range. For large-diameter devices, the current level is also large and the voltage drop on the  $\sim 30 \Omega$  non-scalable resistance becomes significant. Kelvin measurements are carried out on large devices to correct for extrinsic resistance. An average current density of  $4 \text{ MA/cm}^2$  is demonstrated for sub-100-nm devices at  $V_{ds} = 0.3 \text{ V}$ .

The near-ideal nature of our Esaki diodes is further illustrated in **Fig. 10**, which shows that for devices with PVCR  $> 1.5$ , the peak voltage exhibits a rather tight distribution. This is consistent with an Esaki tunneling process that is only determined by the tunneling window which is itself set by the doping level. For devices with low PVCR  $< 1.5$ , the peak voltage is pushed higher due to excess current from non-idealities such as traps.

**Fig. 11** benchmarks average current density at the Esaki peak and at  $V_{ds} = 0.3 \text{ V}$  vs. diameter and vs. effective doping level [8] for state-of-the-art GaSb/InAs Esaki diodes [9, 11-15] and the most advanced TFETs [4]. Our work demonstrates for the first time an Esaki peak current density of  $1 \text{ MA/cm}^2$  at sub-10-nm dimensions (**Fig. 11 (a)**), a territory relevant for future ultra-scale VNW TFET logic applications. Our peak current density is also among the best at our nominal doping level (**Fig. 11 (c)**). As shown in **Fig. 11 (b)**, at  $V_{ds} = 0.3 \text{ V}$ , we achieve a current density of  $4 \text{ MA/cm}^2$ . This is  $> 10\times$  higher current density than state-of-the-art GaSb/InAs VNW TFETs with  $D = 15 \text{ nm}$  [4]. **Fig. 11 (d)** summarizes five criteria for the design and fabrication of high-performance GaSb/InAs Esaki diode and TFETs that our devices fulfill.

#### IV. QUANTUM TRANSPORT SIMULATIONS

The nearly ideal behavior of these devices makes them an excellent testbed for quantum transport simulations. Self-consistent simulations using the Non-Equilibrium Green's

functions (NEGF) formalism with an  $8 \times 8 \text{ k} \cdot \text{p}$  Hamiltonian have been performed [16]. Heterojunctions are described in the real-space Hamiltonian by means of position-dependent  $\text{k} \cdot \text{p}$  parameters [17], using material parameters from [18]. To soften the numerical burden, we adopt the coupled mode-space approach [17, 19]. Tensile strain on the InAs layers is included. Phonon scattering is considered by means of local self-energies in the self-consistent Born approximation [19]. We treat acoustic phonons in the elastic approximation and polar phonons as dispersion-less optical phonon scattering with a phonon energy  $\hbar\omega = 30 \text{ meV}$ .

**Fig. 12 (a)** compares simulated and measured I-V characteristics of a device with D(GaSb) = 11 nm and D(InAs) = 21 nm, where simulations do not account for inelastic phonon scattering. The agreement with experiments is improved by accounting for the series resistance ( $R_s$ ) of this specific device and by introducing a simple expression of the recombination current in the space charge region,  $I_R$ , to better reproduce the Esaki valley current. **Fig. 12 (a)** simulations exhibit a larger current for positive  $V_{ds}$  and a narrower NDR region with a lower peak voltage than the experiments. The inclusion of inelastic phonon scattering improves both above aspects (**Fig. 12 (b)**). In fact, **Fig. 13** shows that for  $V_{ds} = -0.2 \text{ V}$ , phonon emission opens an inelastic tunneling path at the tunneling junction at  $x = 20 \text{ nm}$ , which tends to push the peak voltage higher. For  $V_{ds} = +0.3 \text{ V}$ , **Fig. 14** reveals that phonon emission essentially acts as a diffusive scattering mechanism that degrades the current. Quasi-ballistic transport is observed in (a) plots in **Fig. 12** and **Fig. 13** when deformation potential ( $D_{op}$ ) is small. The still imperfect agreement in the NDR region might be due to band tails from high doping [20] or traps outlining challenges for future simulation efforts.

#### V. CONCLUSIONS

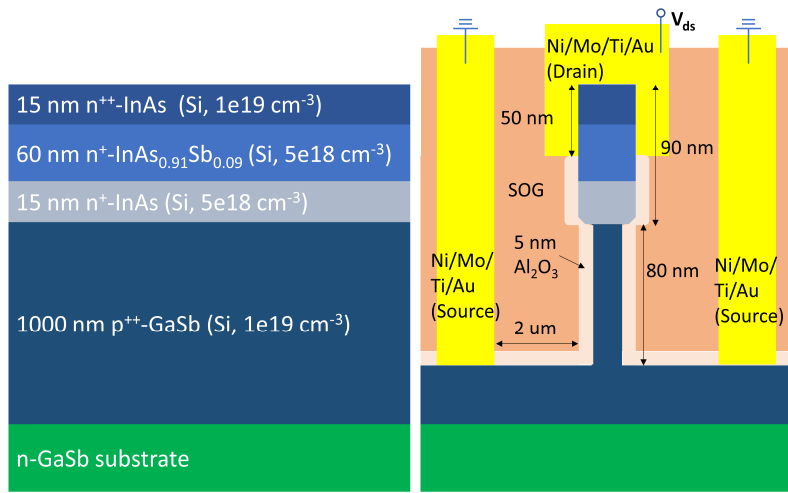
We present the first demonstration of sub-10-nm diameter VNW GaSb/InAs Esaki diodes. The devices exhibit ideal current scaling behavior over nearly two orders of magnitude of diameter. Quantum transport simulations show the important role that inelastic phonon scattering plays in BTBT. Our results clearly demonstrate a high drive current potential for VNW TFETs for future VLSI applications. They also suggest several reasons for the long-lasting mismatch between III-V TFET modeling and experimental demonstrations.

#### ACKNOWLEDGMENT

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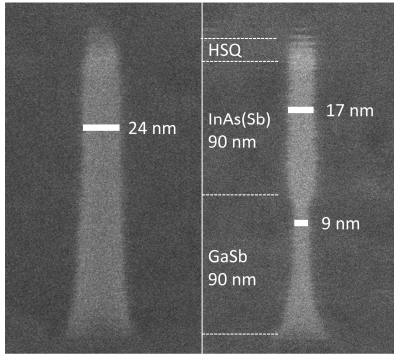


**Fig. 1.** Schematic cross-sectional diagrams of the starting heterostructure and the finished device.

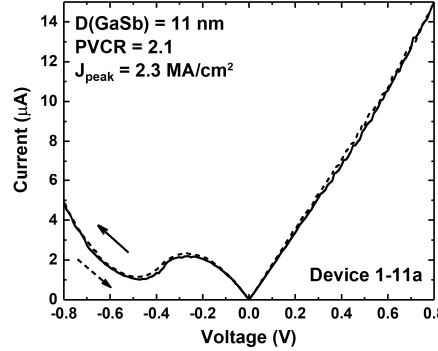
## Process flow

- HSQ hardmask patterning by EBL.
- VNW fabrication by dry etch.
- Alcohol-based digital etch.
- 5 nm  $\text{Al}_2\text{O}_3$  passivation by ALD.
- SOG planarization and etch back (2 times).
- Contact via opening by dry etch.
- $\text{Al}_2\text{O}_3$  removal by TMAH.
- Ni/Mo sputtering for ohmic contact.
- S/D probe pad by Ti/Au lift-off.

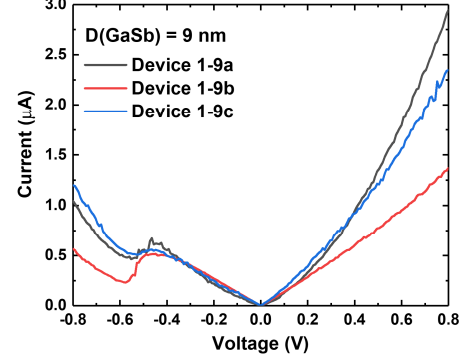
**Fig. 2.** Process flow for GaSb/InAs VNW Esaki diode fabrication.



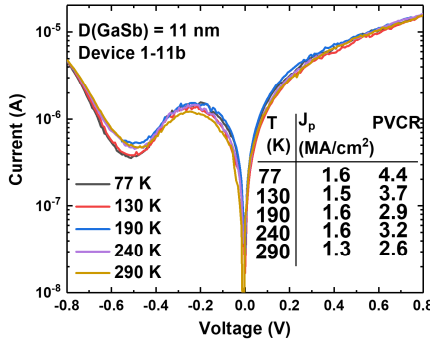
**Fig. 3.**  $D = 24$  nm VNW by RIE (left) reduced to  $D(\text{GaSb}) = 9$  nm (right) after DE.



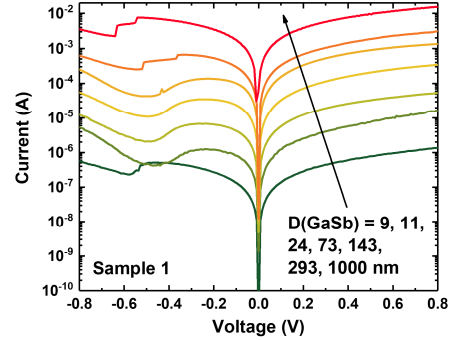
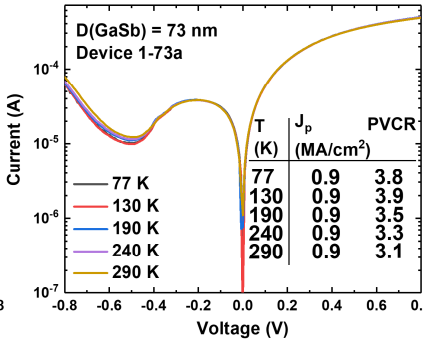
**Fig. 4.** I-V hysteresis sweep of an exemplar  $D(\text{GaSb}) = 11$  nm device from sample 1.



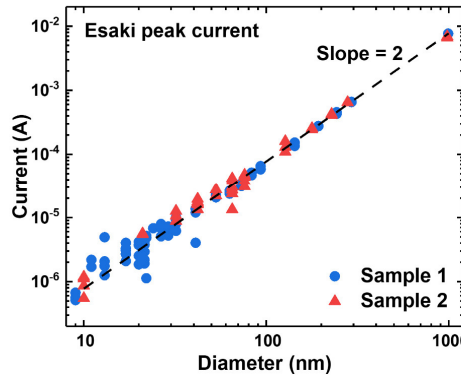
**Fig. 5.** I-V characteristics of three different  $D(\text{GaSb}) = 9$  nm devices from sample 1.



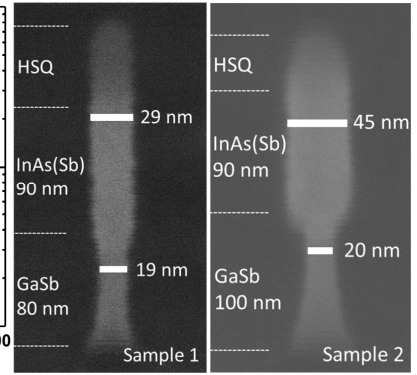
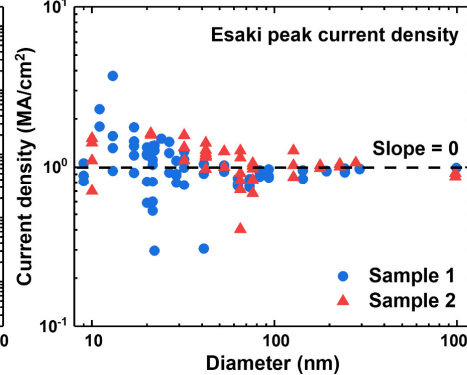
**Fig. 6.** Temperature-dependent I-V characteristics of two devices with different diameters from sample 1. Figures of merit are listed ( $J_p$  stands for peak current density).

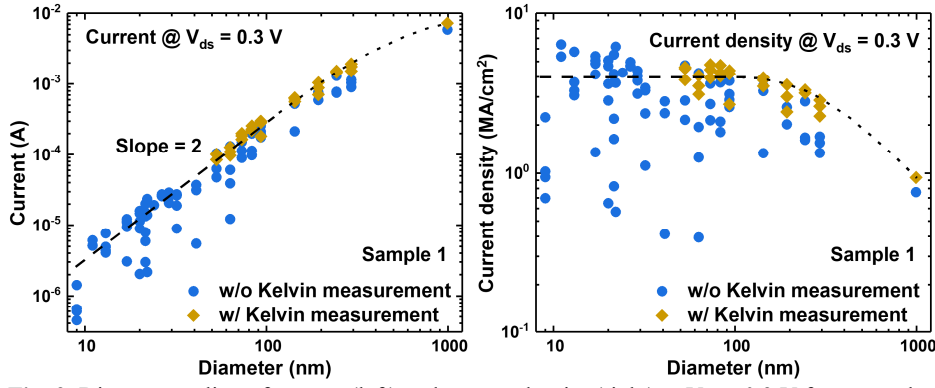


**Fig. 7.** I-V characteristics of devices from sample 1 with different diameters.

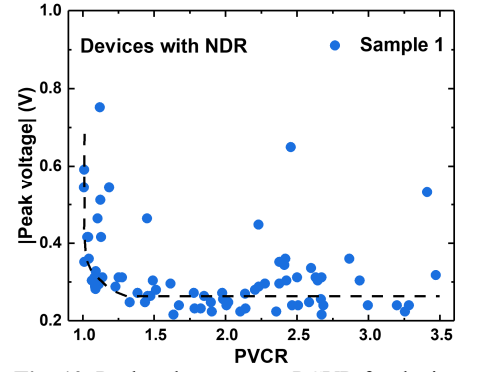


**Fig. 8.** Diameter scaling of peak current (left) and peak current density (middle) from two samples. Dotted lines are a guide for eyes. (Right) SEM images of VNWs with the smallest diameters on the two samples. VNW sidewalls are covered by 10 nm  $\text{Al}_2\text{O}_3$  in total.

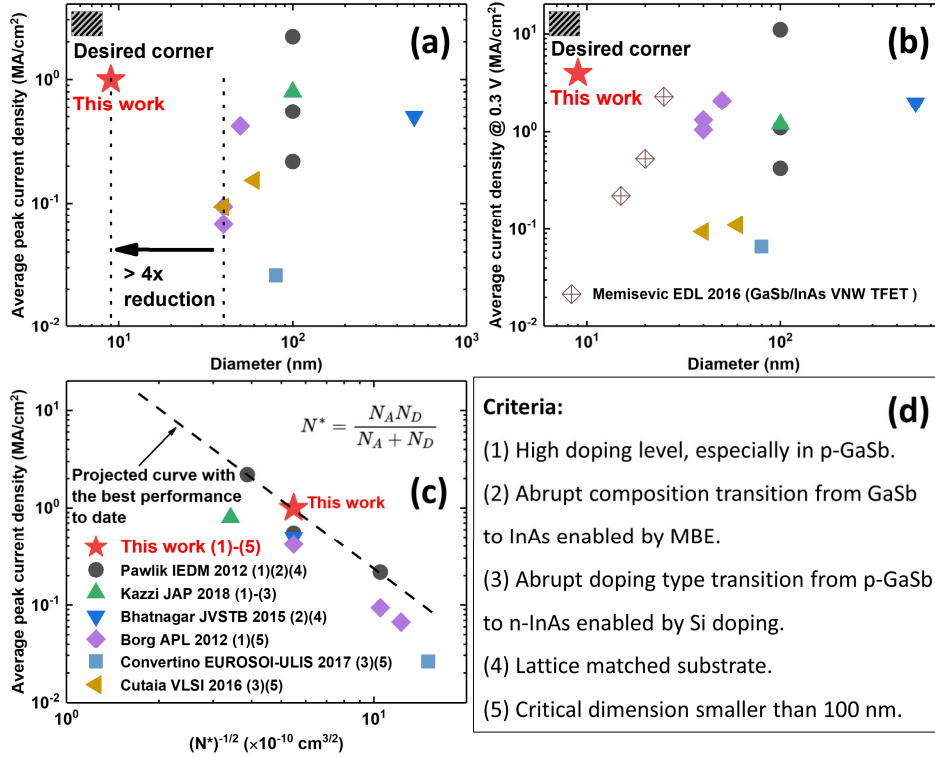




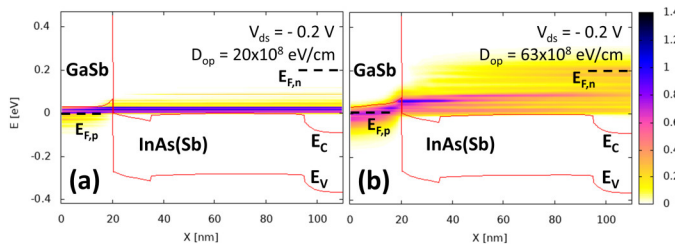
**Fig. 9.** Diameter scaling of current (left) and current density (right) at  $V_{ds} = 0.3$  V from sample 1. Dotted lines are a guide for eyes.



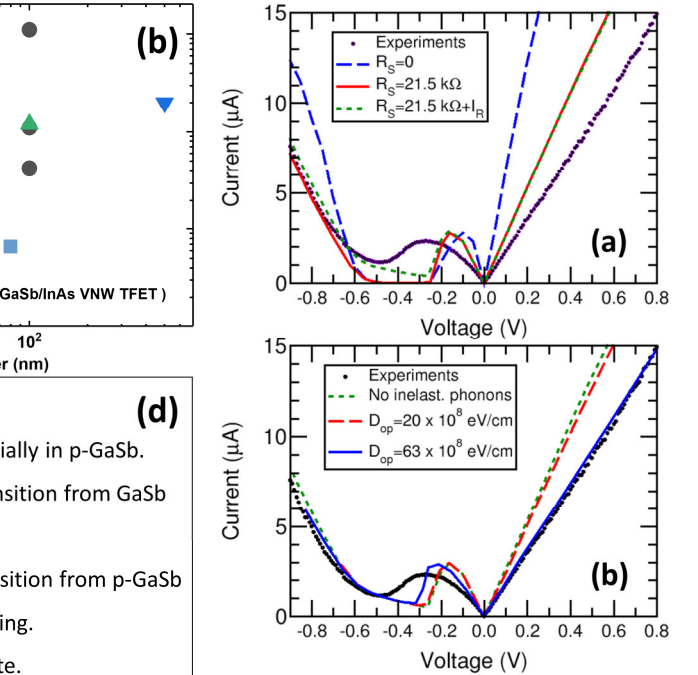
**Fig. 10.** Peak voltage versus PCVR for devices with NDR from sample 1. The dotted line is a guide for eyes.



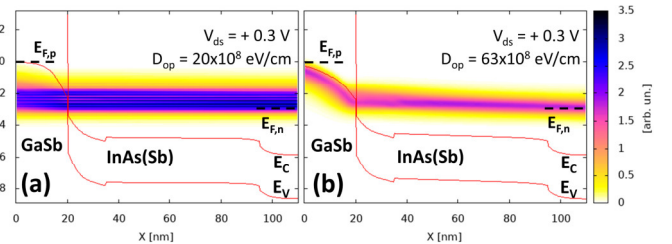
**Fig. 11.** Benchmarks of average peak current density and current density @ 0.3 V vs. diameter and vs. effective doping level for experimentally demonstrated GaSb/InAs Esaki diodes. Criteria for achieving high performance are summarized in the table. Met criteria for each design from the literature are labeled in the legend at the bottom left. Only our work meets all criteria.



**Fig. 13.** Current spectra for the simulations in Fig. 12 (b) at  $V_{ds} = -0.2$  V. (a):  $D_{op} = 20 \times 10^8$  eV/cm. (b):  $D_{op} = 63 \times 10^8$  eV/cm. The energy reference is the Fermi level ( $E_{F,p}$ ) in GaSb, so that  $E_{F,n}$  on the InAs side is given by  $-qV_{ds}$ . The color palette represents spectral current density.



**Fig. 12.** Simulated (lines) and experimental (symbols) I-V curves for the  $D(\text{GaSb}) = 11$  nm device reported in Fig. 4. (a): simulations with and without experimental  $R_s$ , and with/without estimate for recombination current adjusted to reproduce the Esaki valley current. (b): Simulations including  $R_s$ ,  $I_R$  and inelastic optical phonon scattering for different deformation potential ( $D_{op}$ ) values.



**Fig. 14.** Current spectra as in Fig. 13 but for  $V_{ds} = +0.3$  V.