



# Impact of Post-Deposition Anneal on ALD Al<sub>2</sub>O<sub>3</sub>/etched GaN Interface for Gate-First MOSc-HEMT

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## Highlights

- Under 500°C in PDA, Flat band voltage hysteresis ( $\Delta V_{FB}$ ) is reduced in accordance with the reduction of  $GaO_x$  and OH groups
- Over 500°C in PDA,  $\Delta V_{FB}$  increases, due to the increase of  $GaO_x$
- The Fluorine reduction with increasing PDA temperature could explained the decrease of Flat-band Voltage ( $V_{FB}$ )
- $Al_2O_3$  on etched GaN substrate crystallizes for a PDA over 500°C leading to degraded breakdown field

Journal Pre-proof

# Impact of Post-Deposition Anneal on ALD Al<sub>2</sub>O<sub>3</sub>/etched GaN Interface for Gate-First MOSc-HEMT

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**Abstract**— MOS High Electron Mobility Transistors (MOS-HEMTs) may suffer from  $V_{TH}$  instability and hysteresis reducing device performances. Post-Deposition Anneal (PDA) of the Atomic-Layer Deposited (ALD) dielectric has the potential to increase MOS-HEMT performances but needs to be compatible with the actual integration (at CEA Leti : fully recessed Gate First MOS-channel HEMT process flow). In this work, the impact of different PDA temperatures on flat-band voltage ( $V_{FB}$ ) and its hysteresis ( $\Delta V_{FB}$ ) for  $Al_2O_3$  deposited on etched GaN substrates is investigated using MOS capacitors (MOSCAPs). Material properties are analyzed by Hard X-Ray Photoelectron Spectroscopy (HAXPES), Fourier transform infrared spectroscopy (FTIR) and Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) analyses. With increasing PDA temperature up to 500°C: (i)  $\Delta V_{FB}$  decreases and is explained by the reduction of Ga-O bonds at  $Al_2O_3$ /GaN interface and O-H groups in  $Al_2O_3$  (ii)  $V_{FB}$  decreases and could be explained by the reduction of fluorine impurity concentration in  $Al_2O_3$ . For 600°C PDA, Grazing Incidence X-Ray Diffraction (GIXRD) analysis shows a small crystallized  $\kappa$ - $Al_2O_3$  signal on etched GaN contrary to the as-grown GaN. The onset of this crystallization could explain the degradation in breakdown field for PDA above 500°C observed on MOSCAPs after the Gate-First process flow overall thermal budget. Therefore, the optimized PDA temperature suggested for a fully recessed Gate First MOS-channel HEMT is 500°C.

**KEYWORDS:** Post-Deposition Anneal,  $Al_2O_3$ , GaN, MOS, ALD, Hard X-Ray photoelectron spectroscopy

**ABBREVIATIONS:** MOS-channel High Electron Mobility Transistors (MOSc-HEMTs), Hard X-Ray photoelectron spectroscopy (HAXPES), Fourier transform infrared spectroscopy (FTIR), Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS), Grazing Incidence X-Ray Diffraction (GIXRD)

## 1. INTRODUCTION

Due to their two-dimensional electron gas (2DEG) obtained from AlGaIn/GaN heterojunction, GaN based high electron mobility transistors (HEMTs) are interesting for the field of power electronics where higher switching frequency and reduced on-state-resistance ( $R_{on}$ ) [1] are required. HEMTs are normally-on devices with a negative threshold voltage ( $V_{TH} < 0$ ). However, for safety issues and simplified driver systems design, HEMTs with a positive threshold voltage addressed as “normally-off” are highly demanded. One approach is the partial recess of the AlGaIn barrier, increasing  $V_{TH}$  by reducing the 2DEG, but with the drawback of having a  $V_{TH}$  sensible to small variations in the recess depth. To overcome this issue, the MOS-channel HEMT (MOSc-HEMT) with its fully recessed AlGaIn barrier and MOS gate (**Fig. 1**) totally depletes the 2DEG assuring a positive  $V_{TH}$ , and reduces the gate current leakage [2]. Still, its  $V_{TH}$  depends on the gate dielectric  $Al_2O_3$ /etched GaN interface properties [3]. Post-Deposition Anneal (PDA) of  $Al_2O_3$ /GaN has been reported to increase the threshold voltage and reduce its hysteresis ( $\Delta V_{TH}$ ) [4], [5]. Except for Kim et al. [6], most of these reports are for  $Al_2O_3$  deposited either on as-grown or etched GaN substrates using a Gate-Last process flow in which the source and the drain fabrication is carried before the gate fabrication. Since our MOSc-HEMT process flow is Gate-First with a final thermal budget including ohmic contact annealing [7], the impact of  $Al_2O_3$  PDA deposited on etched GaN for the Gate-First process flow is investigated with electrical and chemical characterizations.

## 2. MATERIALS AND METHODS

In order to reproduce the MOSc-HEMT gate processing, 30nm of  $Al_2O_3$  was deposited by Atomic Layer Deposition (ALD) at 300°C using TMA and  $H_2O$  precursors on dry etched nGaIn/Si wafers. The 200mm nGaIn/Si wafers were grown using Metal Organic Chemical Vapor Deposition (MOCVD) on Si substrates, with an GaIn n-type doping of  $5.10^{17} \text{ cm}^{-3}$ . The dry etching was performed using Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) with chlorine-based chemistry. A wet cleaning containing HF was carried out before  $Al_2O_3$  deposition. Since minor consensus is found for PDA's duration, with duration ranging from 30s to 90min [8], [9], a low PDA's duration is performed. Hence, after ALD, PDA was performed under  $N_2$  1) for 4 min at 400, 500, and 600°C on  $1.5 \text{ cm} \times 1.5 \text{ cm}$  samples or 2) for 5 min at 400, 500, and 550°C on 200mm wafers. MOSCAPs test structures were then fabricated: 1) on the  $1.5 \text{ cm} \times 1.5 \text{ cm}$  samples with Au/Ni metal contacts deposited by e-beam evaporation (MOS-1) and 2) on the 200 mm wafers with TiN metal contacts deposited by Physical Vapor Deposition (MOS-2). The MOS-2 devices were annealed after metal deposition to simulate the Gate-First thermal budget including a rapid thermal annealing which was in the temperature range of 400-650°C. The process flows for the two devices are summarized in **Fig. 1**.

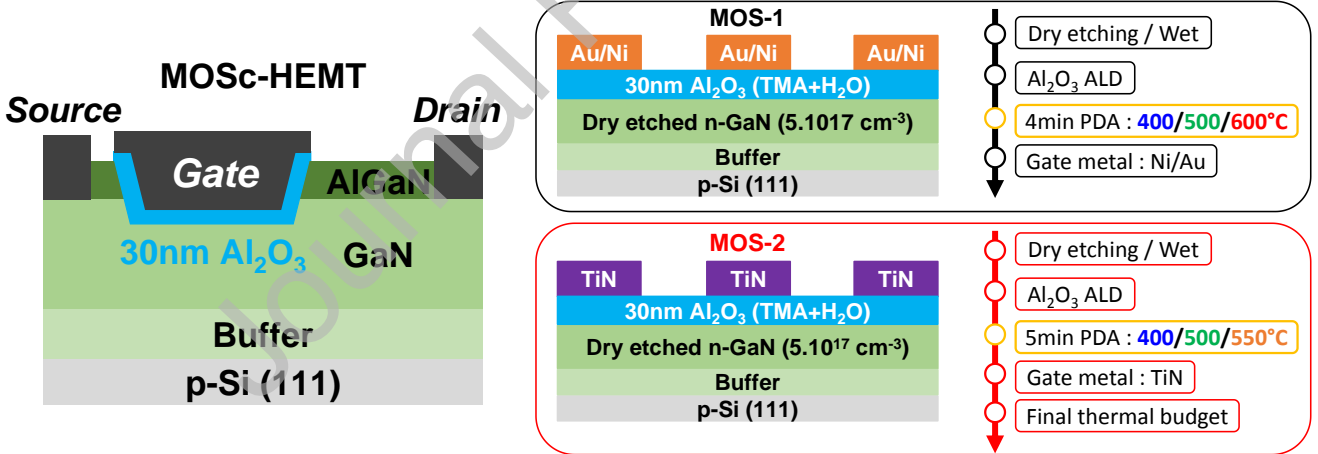


Fig. 1: On the left, the schematic representation of a MOSc-HEMT. On the right, the schematic representation and process flows for MOS-1 and MOS-2

C-V measurements were performed at 1 kHz with a forward voltage sweep from -4V to 6V and backward to -4V using an Agilent 4284A for MOS-1 and using an Agilent B1505A for MOS-2 devices. The flat-band voltage ( $V_{FB}$ ) was extracted using the theoretical flat-band capacitance, which is:

$$C_{FB} = C_{OX}C_D / (C_{OX} + C_D) \text{ with } C_D = \sqrt{kT\varepsilon_{GaIn}\varepsilon_0 / (q^2N_D)}$$

where  $C_{OX}$ ,  $k$ ,  $T$ ,  $\varepsilon_{GaIn}$ ,  $\varepsilon_0$  and  $q$  are respectively the oxide capacitance, the Boltzmann constant, the temperature in Kelvin, the relative GaIn permittivity, the vacuum permittivity and the electron elementary charge. The hysteresis ( $\Delta V_{FB}$ ) is defined as the difference between  $V_{FB}$  in reverse and forward sweeps. Current density-Voltage (J-V) measurements were performed using an Agilent B1505A for MOS-2.

For physical and chemical characterizations, specific  $Al_2O_3$ /GaN samples were prepared with the same processing conditions but with only 15nm of  $Al_2O_3$ . The PDA conditions were the same as for MOS-1 devices. Hard X-Ray Photoelectron

Spectroscopy (HAXPES), Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and Grazing Incidence X-Ray Diffraction (GIXRD) were performed on these dedicated samples. HAXPES analyses were conducted on a PHI Quantes, equipped with both monochromatic Al K $\alpha$  ( $h\nu=1486.7$  eV) and Cr K $\alpha$  ( $h\nu=5414.7$  eV) X-Ray sources, the last one allowing the analysis of buried interfaces. Since the C1s intensity is strongly reduced with a Cr K $\alpha$  source, the binding energy was calibrated with the O1s peak (531.2eV), as measured using the Al K $\alpha$  source and referenced to the C1s peak (284.8eV). The photoelectron take-off angles were set at 45° (Ga2p $_{3/2}$ ) and 90° (O1s) respectively, yielding integrated sampling depths of approximately 16.6 and 24 nm with the Cr K $\alpha$  source. As seen in **Fig. 2a**, three contributions for Ga2p $_{3/2}$  were used: Ga-N (~1117.8eV), Ga-O (~1118.4eV) and Ga-Ga (~1116.5eV). In order to have a comparable analysis, the energy shifts of Ga-O and Ga-Ga with respect to Ga-N were fixed at 0.7eV [10] and -1.3eV [11] respectively. GaN oxidation at the interface was analyzed with the Ga-O area percentage in Ga2p $_{3/2}$  peak. Similarly, O1s peaks were analyzed using O-Al (~531eV) and O-H (~532.2eV) contributions, the energy shift between O-H and O-Al being fixed to 1.2eV [12]. The O1s spectrum with the associated peak fitting is shown in **Fig. 2b**. As for gallium oxide, the presence of O-H groups was deduced from the area of O-H bonds in O1s peak.

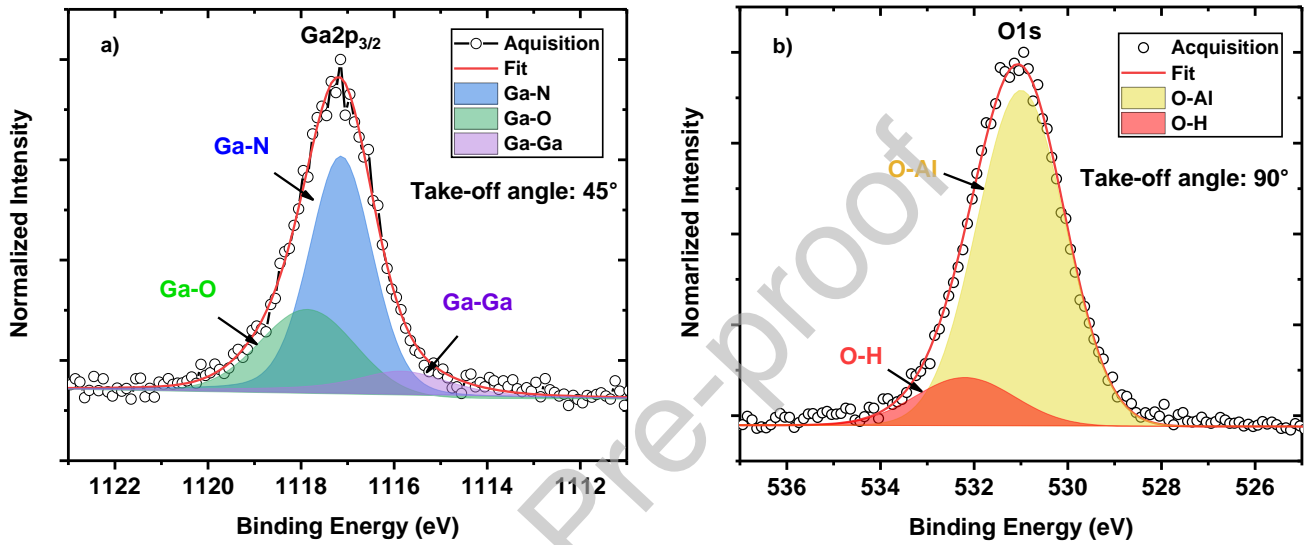


Fig. 2: a) Ga2p $_{3/2}$  spectrum from the reference with a take-off angle of 45°; b) O1s spectrum from the reference with a take-off angle of 90°

ToF-SIMS analyses were performed using a 500eV Cs $^+$  sputter gun and by detecting negative secondary ions. GIXRD was performed with a 2° incident angle and 2 $\theta$  angle between 20° and 60°. Finally, for Fourier transform infrared spectroscopy (FTIR) with multiple internal reflection, dedicated Al $_2$ O $_3$ /Si samples of 30nm Al $_2$ O $_3$  deposited by ALD on p-Si samples were analyzed to study the impact of PDA on OH groups. A manual baseline correction was performed.

### 3. RESULTS AND DISCUSSION

#### 3.1. PDA without final thermal budget

The C-V measurements for MOS-1 devices are reported in **Fig. 3**, with  $\Delta V_{FB}$  and  $V_{FB}$  being extracted and shown in **Fig. 4**.  $\Delta V_{FB}$  is reduced with increasing PDA temperature until a minimum at 500°C, reducing from 108mV to 56mV between the reference and the PDA at 500°C. The reduction of  $\Delta V_{FB}$  with PDA temperature was similarly observed in previous reports [4], [5], [13]. However, for a PDA over 500°C, an increase of  $\Delta V_{FB}$  is observed.

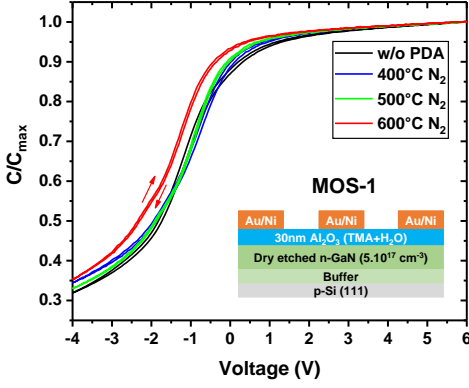


Fig. 3: Normalized C-V characteristics at 1 kHz for MOS-1 devices (median of five measurements)

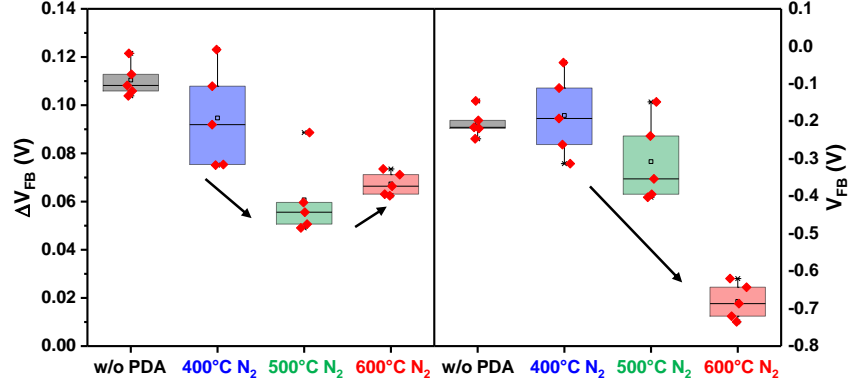


Fig. 4:  $\Delta V_{FB}$  and  $V_{FB}$  for MOS-1 devices extracted from C-V measurements

In the same way, Ga-O bonds observed by HAXPES and related to the presence of interfacial gallium oxide ( $GaO_x$ ) reduce with PDA temperature until 500°C and increase over 500°C (Fig. 5). Since the  $GaO_x$  reduction was reported to reduce hysteresis [14], [15], the reduction of hysteresis with PDA temperature is attributed to  $GaO_x$  reduction at the  $Al_2O_3$ /GaN interface.

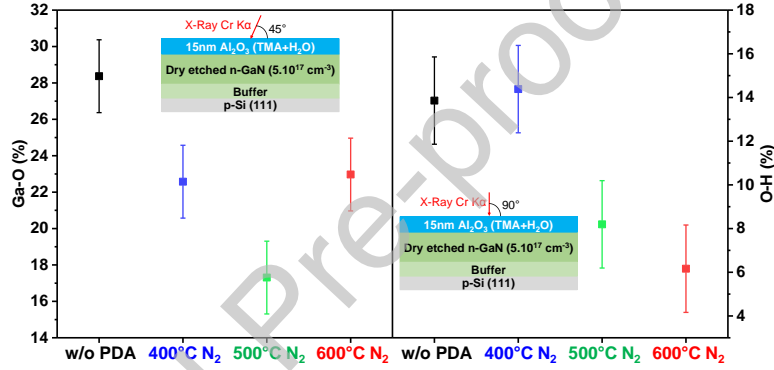


Fig. 5: HAXPES extracted chemical environments (Ga-O and O-H bonds) for different PDA temperatures and without final thermal budget. The take-off angle was 45° for Ga 2p<sub>3/2</sub> and 90° for O1s analysis.

Likewise, OH groups' reduction is observed in  $Al_2O_3$  with increasing PDA temperature. Indeed, OH reduction is confirmed by HAXPES analyses (Fig. 5), as also previously observed by Zhu et al. [16] but with standard XPS. This reduction is also confirmed both by FTIR and ToF-SIMS analyses (Fig. 6). With FTIR, the absorbance spectrum associated to OH bonds reduces and reaches a minimum at 500°C. Through ToF-SIMS, the OH reduction is seen to occur mainly in  $Al_2O_3$  bulk, little reduction at the interface being observed. Specifically, the stretch of OH profile in the GaN substrate for 400°C was also observed for other elements from  $Al_2O_3$  and could be attributed to the impact of surface roughness. Similarly to  $GaO_x$ , the reduction of OH groups was associated with a reduction of hysteresis [14]. As a matter of fact, interstitial hydrogen defect energy levels in amorphous  $Al_2O_3$  were reported to be close to GaN conduction band [17]. This proximity to the conduction band can lead to electron trapping, root cause of the hysteresis. Hence, both reducing OH groups and  $GaO_x$  with increasing PDA temperature until 500°C reduce the hysteresis.



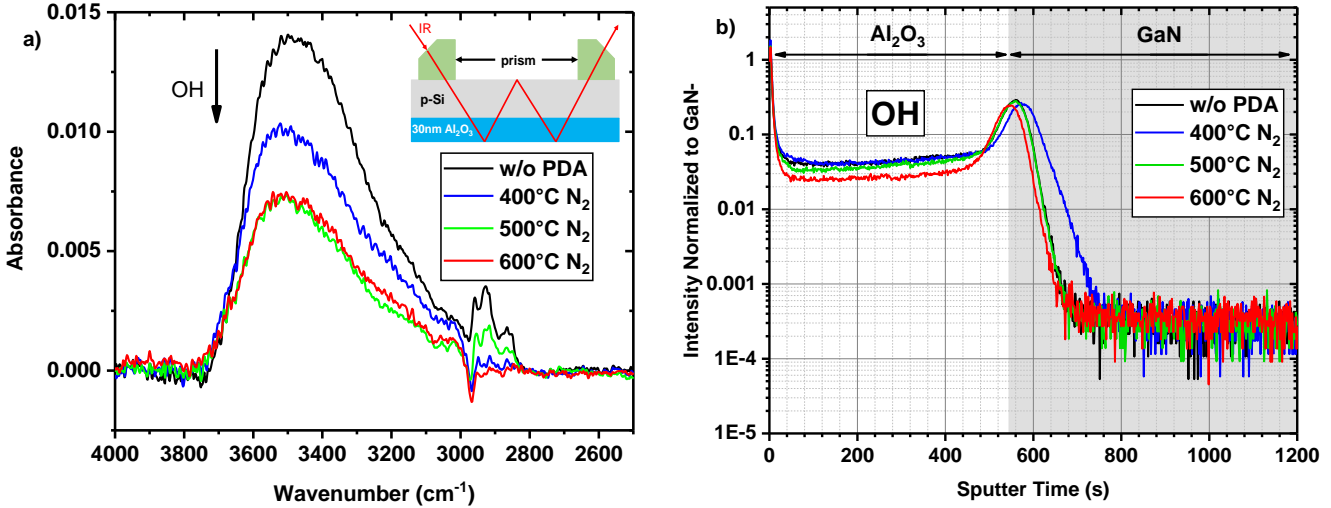


Fig. 6: a) FTIR O-H absorbance spectrum for 30nm  $\text{Al}_2\text{O}_3$  on p-Si with different PDA temperatures and without final thermal budget. A manual correction of base line was performed; b) OH profiles by ToF-SIMS for different PDA temperatures

A small reduction of  $V_{\text{FB}}$  up to 500°C and a strong decrease for a PDA over 500°C is noticed for MOS-1 devices, going from -220mV to -350mV between the reference and the PDA at 500°C and down to -700mV for a PDA at 600°C (**Fig. 4**). The decrease of  $V_{\text{FB}}$  could be detrimental to our MOSc-HEMT, leading to a lower  $V_{\text{TH}}$ . The  $V_{\text{FB}}$  reduction seems to follow the trend of fluorine reduction at the interface observed by ToF-SIMS analyses as reported in **Fig. 7**. Indeed, fluorine profile at the interface reduces with the PDA temperature, with a strong decrease for 600°C. Likewise, the content of fluorine represented by the integrated area under fluorine profile reduces with PDA temperature. A diffusion of fluorine in  $\text{Al}_2\text{O}_3$  bulk region is also observed for a PDA higher than 500°C. As for OH groups, the stretch of fluorine in the GaN substrate for 400°C can be attributed to the surface roughness. The origin of fluorine contamination could be attributed to the wet cleaning containing HF [18]. Since fluorine doping of  $\text{Al}_2\text{O}_3$  is also used to increase  $V_{\text{TH}}$  by introducing negative charges [19], [20], the reduction of fluorine could explain the reduction of  $V_{\text{FB}}$  for MOS-1 devices. Nonetheless, the reduction of  $V_{\text{FB}}$  could also be explained by the increase of positives charges present such as  $\text{V}_{\text{O}}^{+2}$  or  $\text{Al}_i^{+3}$  or the decrease of negatives charges such as  $\text{O}_i^{-2}$  or  $\text{V}_{\text{Al}}^{-3}$  [21], [22].

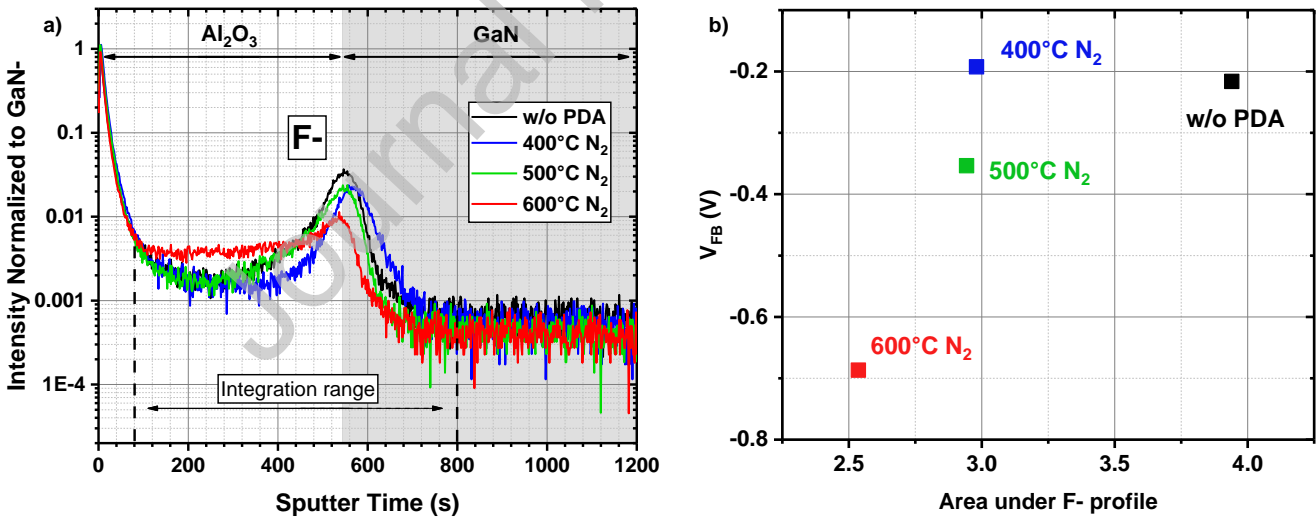


Fig. 7: a) Fluorine profiles obtained by ToF-SIMS for different PDA temperatures; b) Integrated area under fluorine profiles for a defined range as a function of  $V_{\text{FB}}$  for MOS-1 devices.

Hence, without the final thermal budget, a PDA until 500° is beneficial to reduce  $\Delta V_{\text{FB}}$  and limit the reduction of  $V_{\text{FB}}$ . Further increasing the PDA temperature leads to an increased  $\Delta V_{\text{FB}}$  and reduced  $V_{\text{FB}}$ .

### 3.2. PDA with the final thermal budget

In the case of MOS-2 devices having the final thermal budget, the CV measurements are reported in **Fig. 8**, with the extracted  $\Delta V_{\text{FB}}$  and  $V_{\text{FB}}$  shown in **Fig. 9**. The impact of different PDA temperatures is reduced, with  $\Delta V_{\text{FB}}$  being around 20mV for a PDA temperature lower than 500°C (**Fig. 9**). However, a PDA over 500°C induces an increase in hysteresis. On the other hand,  $V_{\text{FB}}$  is

around 1.2V for all PDA temperatures (Fig. 9). Considering that all MOS-2 samples were subject to the final thermal budget, the stable  $V_{FB}$  could be explained by an overall reduction of Fluorine.

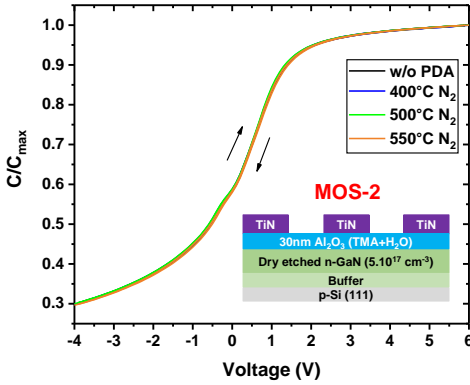


Fig. 8: Normalized C-V characteristics at 1 kHz for MOS-2 devices (median of nineteen measurements)

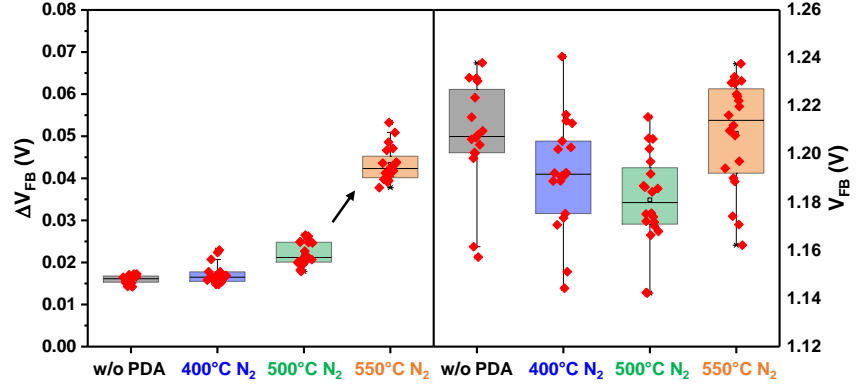


Fig. 9:  $\Delta V_{FB}$  and  $V_{FB}$  for MOS-2 devices extracted from C-V measurements

The difference between MOS-1 and MOS-2 could be attributed to the impact of the final thermal budget. The  $V_{FB}$  is increased (from -0.2 to 1.2 V) and stabilized together with a reduction of  $\Delta V_{FB}$  for PDA under 500°C (from 0.11 to 0.02 V). Further investigation is needed to understand its impact. Indeed, the thermal budget can act as a Post-Metallization Anneal (PMA) on the gate properties, which has been reported to be beneficial [21], [23]. Another difference is the gate metal material and deposition technique, which can affect the  $V_{FB}$ . Indeed, e-beam evaporation was reported to introduce positive charges [24] hence reducing  $V_{FB}$  for MOS-1 devices.

Moreover, the breakdown field extracted from J-E measurements for MOS-2 devices (Fig. 10) is degraded when the PDA temperature is above 500°C, with early breakdown for a given population of devices at 550°C (Error! Reference source not found.). The early breakdown is associated to soft breakdown mechanism whereas the higher breakdown is related to the hard breakdown.

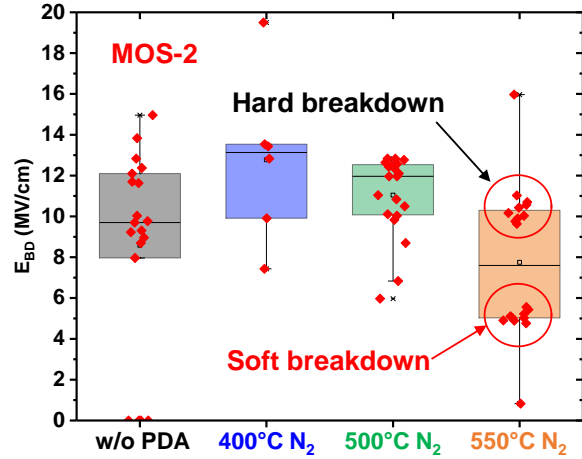
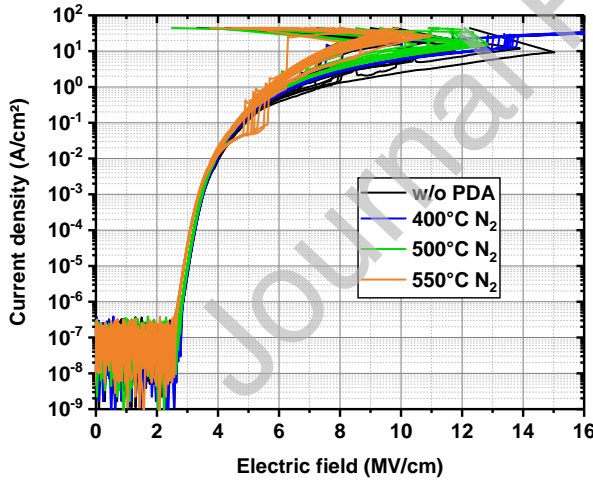


Fig. 11 : Breakdown field obtained from J-E measurements of MOS-2 devices after the final thermal budget.

Furthermore, with GIXRD, the presence of an orthorhombic  $\kappa$ - $Al_2O_3$  peak is observed for a PDA at 600°C and attributed to the (122) plan (Fig. 12). This indicates the beginning of crystallization for  $Al_2O_3$ . The absence of peaks with a PDA at 500°C for etched GaN substrates and with a PDA at 600°C for as-grown GaN substrates confirms that the crystallization onset occurs above 500°C for an etched GaN substrate. The crystallization temperature is lower than the temperature of 850°C reported for ALD  $Al_2O_3$  on etched GaN [6]. This difference could be ascribed to the different cleaning sequence (i.e. TMAH) and different oxidant precursor (i.e.  $O_2$  plasma) as well as the etching process. The GaN etched surface is believed to be the reason for the reduced  $Al_2O_3$  crystallization onset temperature ( $\sim$ 600°C), further consolidating the need for studies on etched substrates, with processing conditions as similar as possible as the actual transistor process flow.

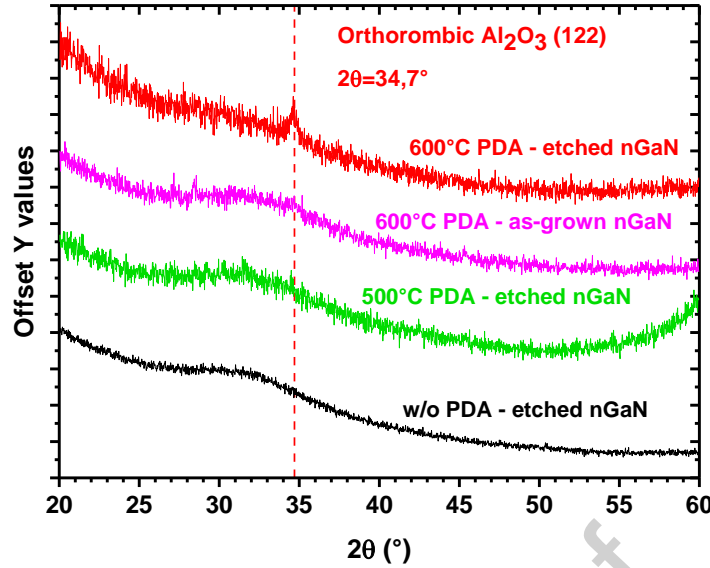


Fig. 12 : GIXRD analysis with grazing angle of  $2^\circ$  for 15nm  $\text{Al}_2\text{O}_3$  on etched GaN without PDA, with a 500°C and 600°C PDA, and for 15nm  $\text{Al}_2\text{O}_3$  on as-grown GaN with a 600°C PDA. All the samples have no final thermal budget.

The observed beginning of crystallization above 500°C can explain the degradation of the breakdown field. Indeed, the formation of grain boundaries can act as current paths resulting to be detrimental for the breakdown field. This observation further consolidates the negative impact of PDA above 500°C for  $\text{Al}_2\text{O}_3$  deposited on etched GaN.

Hence, with the increased hysteresis and degraded breakdown field, the combination of PDA and final thermal annealing is detrimental in the case of PDA temperature over 500°C.

#### 4. CONCLUSION

The impact of PDA for  $\text{Al}_2\text{O}_3$  on etched GaN substrates for Gate-First MOSc-HEMTs process flow was investigated with both electrical and chemical characterizations. In the case of PDA below 500°C without the final thermal budget, the beneficial reduction of hysteresis is observed, correlated to the reduction of  $\text{GaO}_x$  at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface and OH groups in the alumina. A small reduction of  $V_{\text{FB}}$  following the trend of fluorine reduction in  $\text{Al}_2\text{O}_3$  is also observed. However, for a PDA above 500°C, the hysteresis increases likewise linked to the increase of  $\text{GaO}_x$ .

With the device final thermal budget, the PDA's effect on  $V_{\text{FB}}$  is reduced. However, the degradation of hysteresis is equally observed for a PDA over 500°C. Furthermore, a degradation of breakdown field is observed and is explained by the beginning of  $\text{Al}_2\text{O}_3$  crystallization appearing only on etched GaN substrates.

Therefore, the overall thermal budget and the GaN processing prior to  $\text{Al}_2\text{O}_3$  deposition, both influence the impact of PDA; these parameters should be taken into account when optimizing the PDA for the Gate-First approach. The best PDA conditions so far for our MOSc-HEMT architecture seem to be 500°C.

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#### Declaration of interests

☒ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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**Impact of Post-Deposition Anneal on ALD  $\text{Al}_2\text{O}_3$ /Etched GaN Interface in Gate-First MOSc-HEMT**

**Optimum of PDA at 500°C for MOSc-HEMT**

