InGaAs/GaAsP Superlattice Resonant Cavity-Enhanced Photodetector Fabricated on a Nominal Si(001) Substrate for Near- and Short-Wavelength Infrared Applications

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Abstract

The III-V materials offer superior optoelectronic performance that make them an attractive choice for integration into cheap and ubiquitous Si-based technologies, contingent upon addressing the consequences of the prohibitively large lattice constant mismatch between the two material systems. We present a near-infrared resonant cavity-enhanced photodector (RCE PD) monolithically integrated onto a nominal Si(001) substrate and incorporating a thin InGaAs/GaAsP strained-layer superlattice acting as the absorber, as well as five repetitions of GaAs/AlGaAs Distributed Bragg Reflectors providing resonant enhancement. The photodetector was MOCVD-grown onto the Si(001) substrate using a buffer incorporating simultaneously a GaAs bulk layer

and the DBR stack, a two-step growth temperature sequence, and an optimised thermal cycle annealing process, with a total structure thickness of 2.6 µm. The device demonstrates 13-21% internal quantum efficiency against the theoretical maximum of 39%, a result that is easily extendable via addition of DBR pairs or other reflectors. Thanks to the thin absorber design inherent to the RCE PD architecture, the dark current density of the Si-based device is reduced to the same order of magnitude ($\sim 10^{-8}$ A cm^{-2}) as an identical structure grown on a lattice-matched GaAs substrate. In general, the promising structural and optoelectronic results for this structure represent a viable track to direct monolithic integration of III-V materials onto Si wafers, while the tunability of the InGaAs/GaAsP superlattice system opens up the potential for extended NIR and SWIR coverage.

Keywords

NIR, resonant cavity-enhanced photodetector, InGaAs, superlattice, Si(001), MOCVD

1 Introduction

The need for light detection techniques in the near-infrared (NIR) and short-wavelength infrared (SWIR) range of 750 nm to 1.5 µm has become ubiquitous in a number of important sectors and technologies, such as telecommunications, LIDAR,[1] food safety[2,3] and industrial monitoring,[4] agricultural quality control,[5,6] and biomedical diagnostics.[7] Furthermore, the realisation of the concept of the Internet of Things as well as the challenges of transcending Moore's law will necessitate extremely low cost integration of for the proposed detection technologies for them to be viable[8–10] – which, in practice, translates into the requirement of compatibility with the extremely mature Si-CMOS technology. However, while silicon represents by far the most widespread solid state material used for visible light detection, its indirect bandgap of 1.12 eV and relatively low carrier mobilities result in a rather limited

applicability in the NIR region of absorption. In response, III-V group of materials have been growing in relevance as a viable alternative thanks to their direct bandgap allowing for superior responsivity,[11] up to an order of magnitude improvement in carrier mobility,[12] and control over the absorption edge position thanks to tunable alloy compositions. However, due to the severe lattice mismatch between the III-V materials and nominal silicon substrates (eg. 4.5% for GaAs, or 8.4% for the technologically important $In_{0.53}Ga_{0.47}As$ at 300 K), direct monolithic integration on Si has proven a major challenge. Alternative approaches have been developed; native III-V substrates, flip-chip integration,[13] direct or hybrid wafer bonding[14] and epitaxial regrowth[15] have all proven their viability at the cost of increased (and, depending on the target industry, potentially prohibitive) fabrication complexity and costs. As such, interest in direct epitaxial integration has been increasing, with techniques such as bulk and graded buffers,[16,17] dislocation filtering superlattices,[18,19] rapid thermal annealing, or selective area epitaxy[20–24] explored as potential solutions.

This paper reports on the design, fabrication and characterisation of an InGaAs-based resonant cavity-enhanced photodetector monolithically integrated onto a nominal 300 mm Si(001) substrate in an MOCVD reactor, by incorporation of a bulk GaAs buffer layer and an optimised thermal cycle annealing process. The thin absorber is a strain-balanced type-I superlattice with a tunable bandgap,[25–29] comprising alternating InGaAs and GaAsP layers optimised to target the 940 nm wavelength, while 5 repetitions of GaAs/AlGaAs Distributed Bragg Reflectors (DBR) provide resonant enhancement. The device achieves 13-21% internal quantum efficiency, which represents one-third to a half of the maximum achievable theoretical quantum efficiency for this device configuration (39%). In addition, it shows very favourable dark current behaviour with densities comparable to that of a reference GaAs-based device, with only a weak voltage dependence. Thanks to the inherent characteristics of the RCE PD design, the sensitivity of this device could be easily improved while keeping volume-dependent dark current suppressed, while the tunable bandgap of the InGaAs/GaAsP system allows it to be optimised for other wavelengths of interest.

2 Results and discussion

2.1 Design of the InGaAs / GaAsP RCE PD

The signal enhancement and the wavelength selectivity that characterise RCE PDs arises due to the presence of Distributed Bragg Reflectors (DBRs). For the wavelength range of interest, a natural choice of DBR alloys is GaAs/AlAs, as it offers one of the highest III-V refractive index contrasts (∼0.5), is almost lattice matched to GaAs as well as transparent above its absorption edge (870 nm), and has an established epitaxial and process flow.[30–32] In order to reduce oxidation of the highly reactive AlAs mesa sidewalls during processing, about 12% of Ga is added, which has only a negligible effect on the refractive index contrast. As a compromise between device performance and material cost, we choose to have one half of a DBR pair above the cavity (which doubles as the p-GaAs contact layer with the appropriate optical thickness) with a reflectivity of R1 = 0.31 at 940 nm, and optimise the bottom DBR and the active zone thicknesses using the maximum quantum efficiency condition[30] $R_1 = R_2 exp(-2\alpha_{abs} d_{abs})$, where $\alpha_{InGaAs} \sim 9000$ cm^{-1} at the target wavelength; this results in bottom reflectivity $R_2 = 0.41$, most closely matched by 5 GaAs/AlGaAs DBR pairs (R∼47%), and $d_{InGaAs} \sim 155$ nm.

A III-V ternary alloy such as InGaAs offers the technologically attractive property of a continuously varying bandgap and therefore absorption edge, however lattice matching to the substrate/buffer requires careful management. On GaAs, the Matthews-Blakeslee[33] critical thickness (h_c) of $In_{0.13}Ga_{0.87}As$ is 56 nm at room temperature, and 59 nm at the growth temperature of 580°C; as such, in order to avoid formation of threading dislocations (TDs), a strain-balancing layer of GaAsP is introducted to form what is effectively a type-I strained-layer superlattice (SLS). At the appropriately chosen composition and thickness, an addition of a thin layer of GaAsP to the InGaAs quantum well can minimise the average-in plane stress of the two layers,[34] effectively extending the critical thickness of the resultant superlattice to an arbitrary value. For this particular structure, a 12 nm of $In_{0.13}Ga_{0.87}As$ and 8 nm of

$GaAs_{0.62}P_{0.38}$ are chosen to provide approximately equal and opposite cumulative strains; this also results in an InGaAs quantum well that is relatively shallow (with a conduction band offset of 220 meV and a valence band offset of 300 meV), which aids in photocarrier extraction.[35] The resultant superlattice absorber is then sandwiched between a Zn-doped ($\sim$1x10^{19} cm^{-3}) p-GaAs top contact with an optical path length thickness (OPL) of $\lambda/4$ = 67 nm, and a Si-doped ($\sim$2x10^{18} cm^{-3}) n-GaAs with an OPL of $3\lambda/4$ = 206 nm. This forms a standard photodiode structure which can be grown directly onto the DBR stack, as shown in Figure 1.

2.2 Fabrication

Two RCE PDs were grown entirely in-situ using an Applied Materials MOCVD reactor: a reference device on a lattice-matched 100 mm n-type GaAs substrate, and a Si-based device on a nominal 300 nm industry standard n-type Si(001) wafer miscut at 0.15°. The Si surface was prepared for growth in situ using a SiCoNi™oxide removal dry cleaning process; this was then followed by a near-atmospheric pressure annealing process at 800-900°C under H_2 flow to enable antiphase domain (APD) removal during the subsequent GaAs buffer layer growth.[36] Then, a $\sim$1.4 µm GaAs buffer layer was deposited using trimethylgallium (TMGa) and tertiarybutylarsine (TBAs) sources and ultrapure H_2 as the carrier gas, in a two-step growth method wherein a thin GaAs nucleation layer was first grown at a temperature low enough to limit adatom diffusion length (370°C), subsequently followed by a high-temperature (640°C) GaAs growth with annealing properties. This was then terminated by a short GaAs deposition step at the standard growth temperature of 620°C, after which the five $Al_{0.88}Ga_{0.12}As$/GaAs DBR repetitions were grown at the same temperature with the addition of trimethylaluminium (TMAl), followed with the final GaAs layer grown to 206 nm thickness and n-doped using a disilane source. Following the deposition of the DBR stack and most of the n-GaAs contact, a cycle of four repetitions of a thermal cycle annealing (TCA) process was implemented, consisting of a temperature ramp up to 760°C

under low As flux followed by a 5 minute bake, then a cooldown to 400°C and subsequently 350°C with the group V flux switched off. The stack was then capped with the remaining thickness of the n-GaAs layer, after which the intrinsic active zone of 13 repetitions of the $In_{0.13}Ga_{0.87}As$ / $GaAs_{0.62}P_{0.38}$ superlattice is grown, using tertiarybutylphosphine (TBP) and [3-(dimethylamino)propyl] dimethyl indium (DADI). The growth temperature was alternated between 620°C for GaAsP layer and 580°C for InGaAs growth. InGaAs/GaAsP interface quality was assessed during calibration runs by measuring the full-width-at-half-maximum of photoluminescence and X-ray coupled scan spectra. The best results were achieved with a 40 s growth interruption during the temperature ramping from 580°C to 620°C separating the InGaAs and GaAsP growth steps, under TBAs and TBP partial pressures. Finally, to complete the stack, the p-contact / half-mirror GaAs layer was grown with a with Diethylzinc (DEZn) flux acting as the p-dopant.

In addition to the RCE PDs outlined above, an identical structure was grown on a double side-polished N^+-GaAs wafer to enable spectroscopic transmission measurements. A stack of 5 DBR repetitions without the cavity as well as a mirrorless cavity were also grown on identical substrates for the same purposes.

The cavity region was processed into standard architecture p-i-n photodiodes with a diameter of 840 µm in order to enable optoelectronic characterization. The process flow uses photolithography to define the device features, dry plasma etching to define circular mesas down to the n-GaAs contact, and thermal evaporation of ohmic Ti/Au contacts. No anti-reflective coating or chemical passivation steps were applied to the structures.

2.3 Structural characterisation

The material quality of the two RCE PDs was assessed using Atomic Force Microscopy (AFM), X-ray Diffraction (XRD) spectrometry, Focused Ion Beam-Scanning Electron Microscopy (FIB-STEM), and electron channeling contrast imaging (ECCI) methods. Representative 10 µm x 10 µm AFM scans, obtained on a Bruker Dimension Icon system, can be

seen in Figure 2. Unsurprisingly, the structure grown on the lattice-matched GaAs substrates (Figure 2a) shows an extremely low RMS roughness of ∼0.1 nm, as well as the characteristic atomic steps of the underlying substrate surface. The Si/GaAs RCE PD (Figure 2b) has an RMS roughness of 3.5 nm, an increase is mostly attributable to the highly reactive Al atoms clustering around already existing dislocations.

High Resolution X-ray Diffraction measurements were performed on a Bruker JV-DX metrology system, in the form of 004 (symmetric) coupled ($\omega - 2\theta$) scans, as well as 224 (asymmetric) reciprocal space maps (RSM). The $\omega - 2\theta$ scan of the GaAs-based RCE PD, shown in Figure 3a), reveals two sets of sharp periodic peaks: the DBR stack clustered around the substrate peak, and the SLS, whose periodic spacing confirms the presence of 12 nm of InGaAs and 8 nm of GaAsP in the structure. The secondary Pendellösung fringes visible between the primary ones in the SLS peak set are sharp enough to discern the minima (whose n+1 corresponds to the total number of periods), confirming good interface quality. Nevertheless, a very low degree of superlattice relaxation is observed in the form of shoulders on the peaks, which could potentially be attributed to uncompensated strain present in the superlattice at growth temperatures. Reciprocal space mapping around the 224 plane is also included in Figure 3a), again revealing good quality epitaxy. Figure 3b) shows the same measurements for the RCE PD on Si/GaAs. The derived superlattice layer thicknesses are d_{InGaAs} = 11 nm and d_{GaAsP} = 8 nm, relatively well-matched to those of the GaAs RCE PD. The GaAs buffer layer peak is offset from its bulk Bragg angle by ∼200 arcseconds, indicating that the layer is under 1570 ppm of tensile strain owing to the large mismatch in thermal expansion coefficient between GaAs and Si. Peak broadening due to the highly mismatched metamorphic growth on the GaAs buffer causes the disappearance of both the closely packed DBR peaks as well as of the secondary oscillations of the SLS; a broader intensity distribution along the Q(110) axis of the corresponding 224 RSM also points to increased layer TD-induced mosaicity.

Focused Ion Beam-Scanning Electron Microscopy (FIB-STEM) was employed to directly

image the cross-section of the RCE PD structures prepared using Ga ion beam milling. The resultant Bright-Field (BF) image of the GaAs-based device can be seen in Figure 4; no defects are observed at the scale of the measurement, and the interfaces are found to be clean and sharply defined.

The BF-STEM image of the Si-based device (Figure 5a), meanwhile, shows presence of threading dislocations mainly at the Si-GaAs interface and in the following GaAs buffer layer; importantly, however, relatively few of the TDs penetrate into the active zone of the detector or are seen to originate above the buffer layer. No APDs are observed. The undulations in the AlGaAs layers possess spatial periods at the scale comparable to those observed on the AFM surface profiles (see Figure 2b), and can be once again attributed to the low diffusion of Al adatoms preserving the underlying defect morphology.[37,38] It can also be noted that the roughness aggregated by AlGaAs layers is then partly compensated for during the epitaxial growth of the Al-free p-i-n structure on top, as seen in Figure 5a).

To gain a quantitative estimate of dislocation densities, Electron Channeling Contrast Imaging (ECCI) was carried out on the surface of the Si/GaAs RCE PD (Figure 5b) showing the presence of threading dislocations with a density of $\sim$6x10^8 cm^{-2}. This represents a good result for the thickness of the buffer given that no graded layers or dislocation filtering superlattices were employed. A very limited number of stacking faults (SF) was also observed, giving a tentative estimate of $\sim$6x10^6 cm^{-2}.

2.4 Optoelectronic characterisation

Reflectivity (R) and transmission (T) in the NIR region were characterized using a Cary 7000 universal measurement spectrometer. Reflectivity was obtained at 7° angle of incidence (AOI), at which variation from 0° AOI as well as polarization effects remain negligible. Reflectivity collected for 5 pair DBR structures grown on GaAs native substrate and on the Si/GaAs buffer system can be seen in Figure 6a), showing a stopband with R$\sim$77% at its peak, which represents an offset of about 3% from the model prediction (derived from

Fresnel equations implemented using a transfer matrix method[39]). Importantly, the AlGaAs interfacial oscillations in the Si-based DBR do not appear to degrade the total reflectivity as compared to the GaAs-based DBR.

In order to directly evaluate the increase in absorption in the superlattice due to the presence of the DBR stack, the same RCE PD structure (Figure 1) is regrown on a double-side polished N^+-GaAs substrate which prevents scattering of the light off the back of the wafer. Measuring reflectivity R and transmission T then allows to obtain absorption (A) simply via A = 100% - R – T.

A cavity-only sample without the DBR stack was also grown and characterized, as well as a bare n-GaAs substrate. The resultant absorption spectra, corrected for air-GaAs interface reflection, can be seen in Figure 6b). The resonant cavity enhancement is immediately observable at a peak near 943 nm in the RCE PD, accompanied by a commensurately lower absorption feature in the spectrum of the cavity-only wafer. Both can be normalized to the n-GaAs absorption spectrum to account for free carrier absorption in the substrate, which results in $A_{\text{RCE PD}} = 39\%$ and $A_{\text{cavity}} = 14\%$; This corresponds to an enhancement factor of 2.8, which also enables an easy comparison with the maximum obtainable internal quantum efficiency:[30]

$$\eta = \frac{(1 + R_2 e^{-\alpha d})}{1 - 2\sqrt{R_1 R_2} e^{-\alpha d} + (1 - e^{-\alpha d}) R_1 R_2 e^{-2\alpha d}} \tag{1}$$

Where the theoretical values are $\alpha d(\text{InGaAs}) = 0.14$, $R_1 = 0.31$ (the air-GaAs interface), and $R_2 = 0.43$ for the RCE PD (bottom DBR reflectivity after accounting for 3% losses) and 0 for the cavity-only structure. This results in $\eta_{\text{RCE PD}} = 39\%$ and $\eta_{\text{cavity}} = 13\%$, in an excellent agreement with the spectrometric data.

Micro-photoluminescence (µPL) measurements at room temperature were carried out using a Horiba Labram HR system and a diode-pumped 633 nm solid state laser at low power (0.16 mW) in order to avoid peak blueshift due to band filling. Figure 7a) features µPL spectra for both RCE PDs obtained under the same conditions and normalized to unity. The GaAs-based RCE PD displays good quality optical behavior, with a sharp onset of fundamental

absorption along with minimal presence of an Urbach tail and a very low FWMH of 25 meV. The fundamental peak wavelength is found to be at 967 nm; higher level transitions can also be observed above 900 nm. Notably, the Si/GaAs-based RCE PD also shows good quality features when compared to the GaAs lineshape: clear fundamental absorption onset (albeit with a non-negligible sub-bandgap tail) and a decent FWMH = 66 meV of the fundamental peak.

To find the actual fundamental bandgap from the luminescence data, the first derivative of the intensity as a function of energy is calculated (Figure 7a) inset); here, the position of the peak represents the position of the highest rate of change in the joint optical density of states ie. the bottom of the fundamental bandgap;[40] this is found to be 1.276 eV for the GaAs-based RCE PD and 1.283 eV for the Si/GaAs one, a minor shift likely attributable to inhomogeneous indium incorporation across the 300 mm Si wafer. The redshift of the emission peaks with respect to their absorption counterparts in the spectrometric data (Figure 6), meanwhile, can likely be attributed to a disorder-induced Stokes shift.[41,42]

A cursory comparison can be made with a simple Schrödinger 1-band model (Figure 7b), especially the fundamental transition, calculated at 1.30 eV (e1-hh1) with an interband matrix element of P$\sim$0.96, and 1.37 eV (e2-hh2) with an interband matrix element of 0.86.[35] The latter energy corresponds to a wavelength of $\sim$905 nm and is likely partly responsible for the energetic tail present at lower wavelengths, which itself is a convolution of such factors as other energetic transitions with low interband matrix elements, as well as local inhomogeneities in crystal structure.

Dark current measurements (I-V) on the processed photodiodes were carried out using a standard two probe method. In addition, spectrally resolved photocurrent densities above the absorption edge of GaAs were obtained with the use of a 450 W xenon lamp equipped with a Horiba-Jobin Yvon Czerny-Turner monochromator and an optical fibre; a Newport-1830R optical power meter was used to calibrate the optical power incident at the device position. A side-by-side comparison of the dark current density (J_d) and photocurrent den-

sity (J_{ph}) at 930 nm for the two structures can be seen in Figure 8. Remarkably, the actual values of J_d are almost the same near zero bias; this indicates that the elevated TDD present in the neutral regions of the Si/GaAs nevertheless does not contribute significantly to the defect-dependent (Shockley-Read-Hall, or SRH) diffusion current originating in the neutral regions of the diode.[43] The voltage-activated drift current generated through the SRH mechanism can nevertheless be discerned in the Si/GaAs device, however the relatively low (up to about 1 order of magnitude at -3 V) difference between the two structures demonstrates the crucial role of the small absorber volume in an RCE PD in limiting the volume-dependent SRH currents that tend to limit photodiode performance.

The photocurrent densities at 930 nm and under 9x10^{-7} W mm^{-7} of incident optical power (uncorrected for reflectivity) saturate almost immediately under negative bias, pointing towards efficient photocarrier collection. That this is also the case for the relatively high-TDD Si/GaAs RCE PD demonstrates the role that the minimisation of the photocurrent path plays in restoring optoelectronic performance of Si-based III-V devices.

External quantum efficiency was calculated from spectrally resolved photocurrent data and corrected for air-GaAs interface reflection to obtain internal quantum efficiency (IQE), and can be seen in Figure 9a) as a function of incident wavelength. Resonant enhancement is evident for both structures. The GaAs RCE PD reaches 30-35% IQE at 930 nm, close to the 39% predicted by Equation 1 and derived from the spectrometric data (Figure 6). The Si/GaAs RCE PD, meanwhile, achieves IQE values between 13 and 21%. Importantly, this corresponds to 33 to 54% of the maximum achievable IQE, in a further demonstration of the advantages of the RCE PD architecture in efficient carrier collection for highly lattice-mismatched systems. The significance of this result is that the IQE of the device can be easily and predictably improved via an increase in number of the GaAs/AlGaAs DBR pairs, without necessitating additional complex defect engineering solutions. Both devices betray similar, limited voltage dependence up to 0.5 V of negative bias, pointing to some photocarrier losses unrelated to material defectivity and more likely explainable by inbuilt

potential barriers at the superlattice-GaAs contact interfaces. This could potentially be addressed with graded InGaAs interfaces if lower operational voltage is desired. The shift from the target wavelength of 940 nm is easily addressable with pre-growth calibration of the AlGaAs/GaAs growth rates to ensure precise DBR thickness control.

3 Conclusions

A high-performance resonant cavity-enhanced photodetector based on a novel, tunable superlattice system and operational in the NIR region has been monolithically integrated onto a fab-compatible nominal Si substrate using a 300 mm-compatible MOCVD reactor. Simultaneously, an identical structure was fabricated on a lattice-matched GaAs substrate as a reference. The direct integration of the highly mismatched III-V structure onto Si was achieved using an in-situ anneal process to ensure APD-free growth, followed by a two-step growth of a 1.4 µm GaAs buffer layer and terminated with a thermal cycle annealing after the GaAs/AlGaAs DBR stack deposition. The Si-based detector demonstrated a very favourable internal quantum efficiency of 13 to 21%, or between one-third and a half of the theoretical maximum IQE of 39% calculated for this device design. This result is particularly promising as a desired improvement in performance can be easily achieved by an increase in number of GaAs/AlGaAs Distributed Reflector Pairs, rather than a commensurate increase in the absorber volume and the associated volume-dependent dark current components. The merit of low absorber volume in a highly strained system is further demonstrated by the dark current density of the Si-based device, which falls within an order of magnitude of the reference GaAs-based one despite a threading dislocation density of $\sim$6x10^8 cm^{-2} found at the surface. At the same time, the strain-balanced InGaAs/GaAsP superlattice structure is used to prevent further relaxation within the thin active layer; and because of the parameter space inherent to this superlattice system, there exists also a prospect of extending the sensitivity of this type of absorber into the SWIR region. The good material quality of

the Si-based photodetector is further confirmed with an array of structural characterization and microscopic imaging. In general, the proposed RCE PD represents a viable pathway to direct, monolithic integration of high-performance III-V materials onto nominal Si wafers, raising the prospect of significant time and cost savings in photonic circuit integration.

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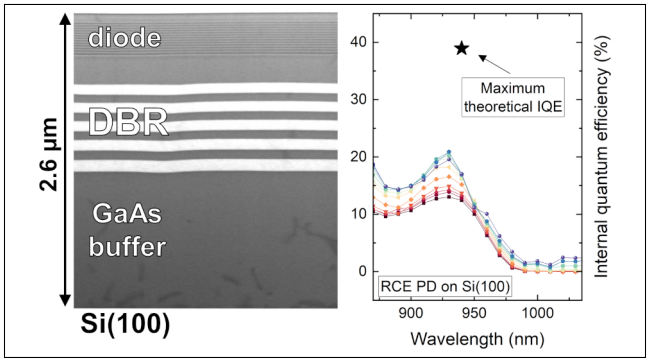
TOC Graphic


diode
DBR
GaAs
buffer
2.6 µm
Si(100)
Maximum
theoretical IQE
RCE PD on Si(100)
Internal quantum efficiency (%)
Wavelength (nm)
40
30
20
10
0
900
950
1000

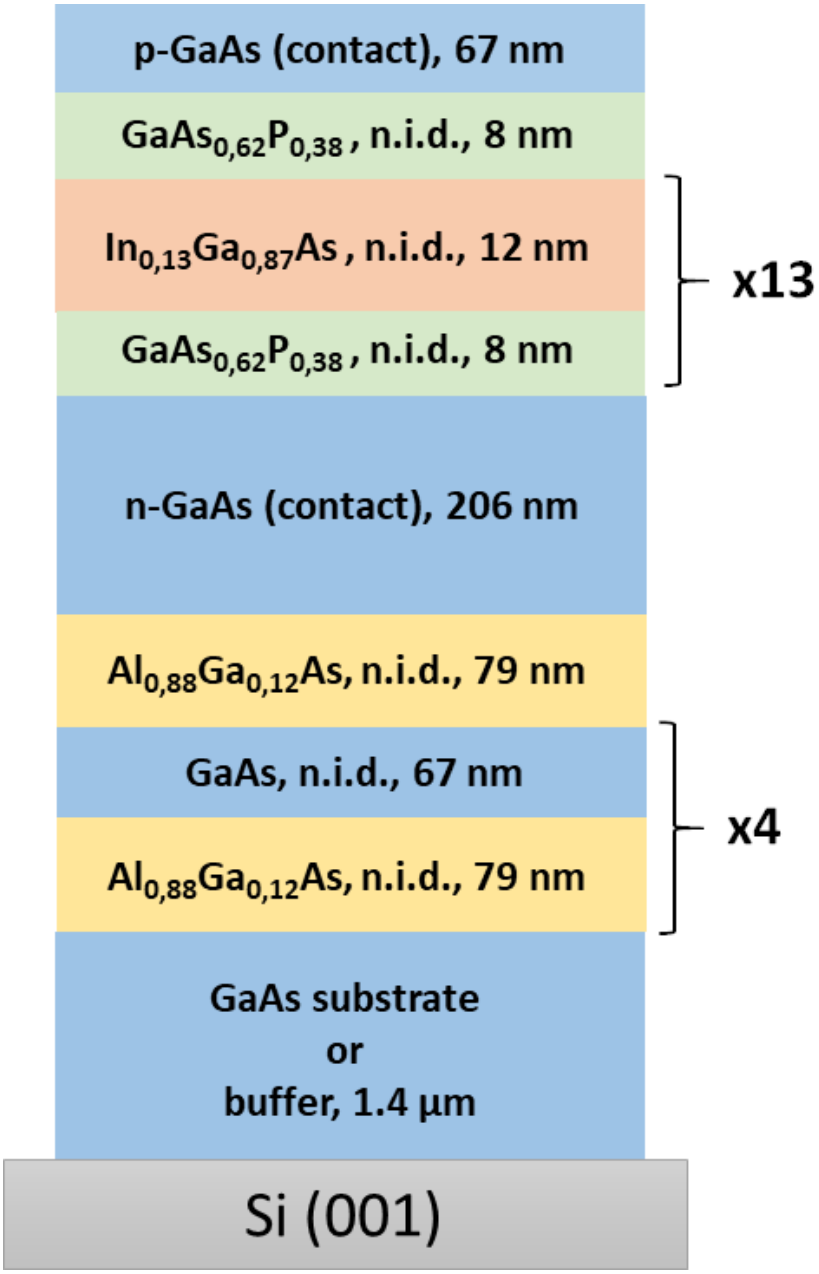


Figure 1: Structure of the InGaAs/GaAsP RCE PD. Here, 'n.i.d.' stands for not intentionally doped.

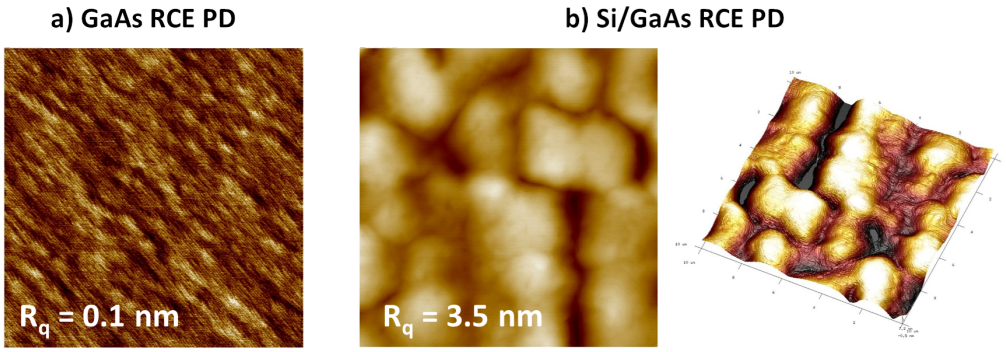


Figure 2: Atomic Force Microscopy Images of the two photodetector structures. a) GaAs RCE PD; b) Si/GaAs RCE PD.

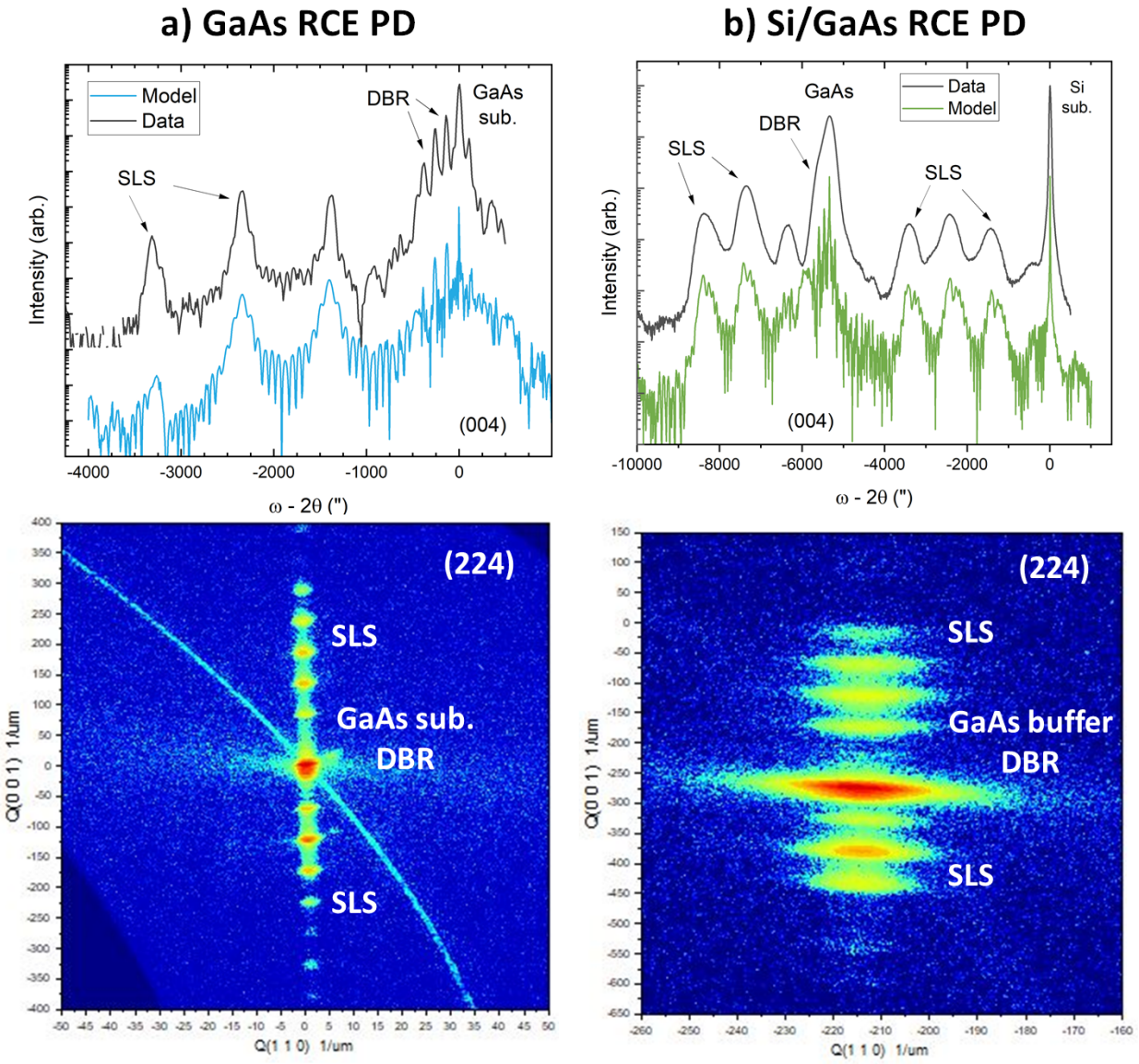


Figure 3: X-ray Diffraction scans in the symmetric $\omega - 2\theta$ 004 configuration (top) and asymmetric 224 reciprocal space maps (bottom) for: a) GaAs RCE PD; b) Si/GaAs RCE PD.

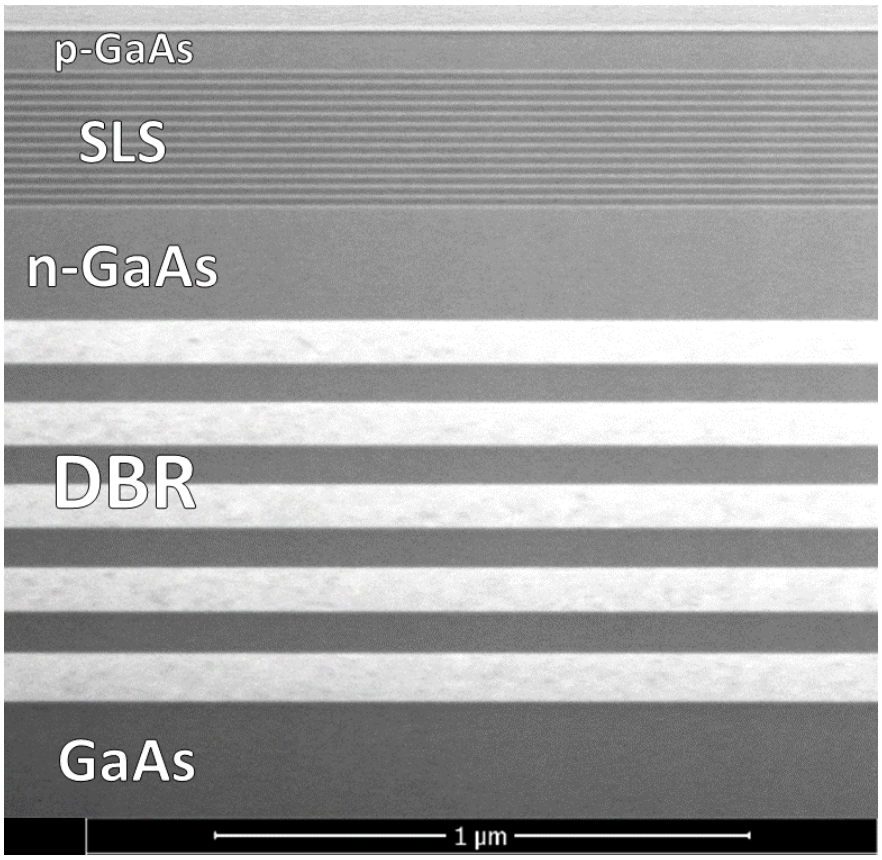


Figure 4: Bright-Field Scanning Transmission Electron Microscopy image of the GaAs RCE PD.

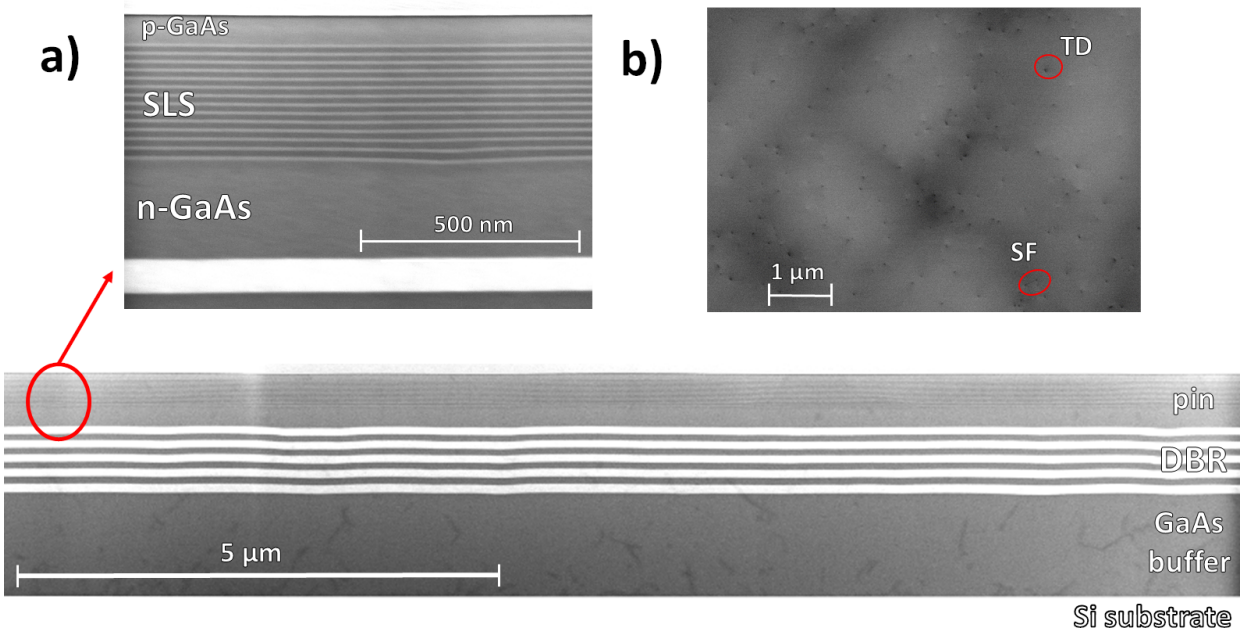


Figure 5: Scanning Electron Microscopy imagery of the Si/GaAs RCE PD. a) Bright-Field Scanning Transmission Electron Microscopy; b) Electron Channeling Contrast Image of the surface, with the example of a threading dislocation (TD) and a stacking fault (SF) circled in red.

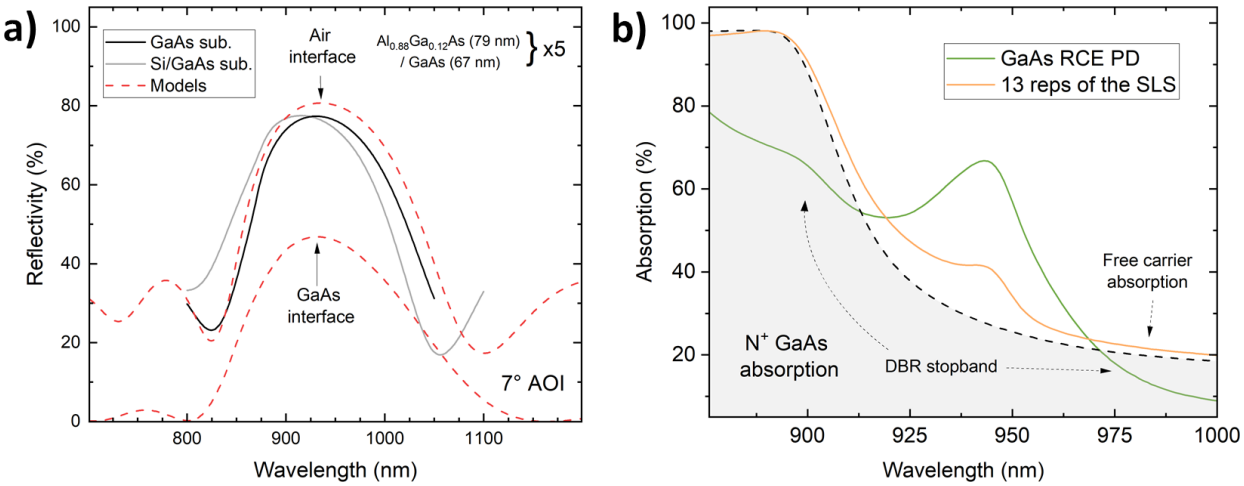


Figure 6: Spectroscopy of the DBR and RCE PD stacks. a) Reflectivity of 5 GaAs/AlGaAs DBR repetitions on GaAs and Si/GaAs substrates, compared to the modelled spectra. b) Absorption spectra for the full GaAs-based RCE PD compared to a cavity-only stack containing 13 repetitions of the superlattice, and the N^+-GaAs substrate.

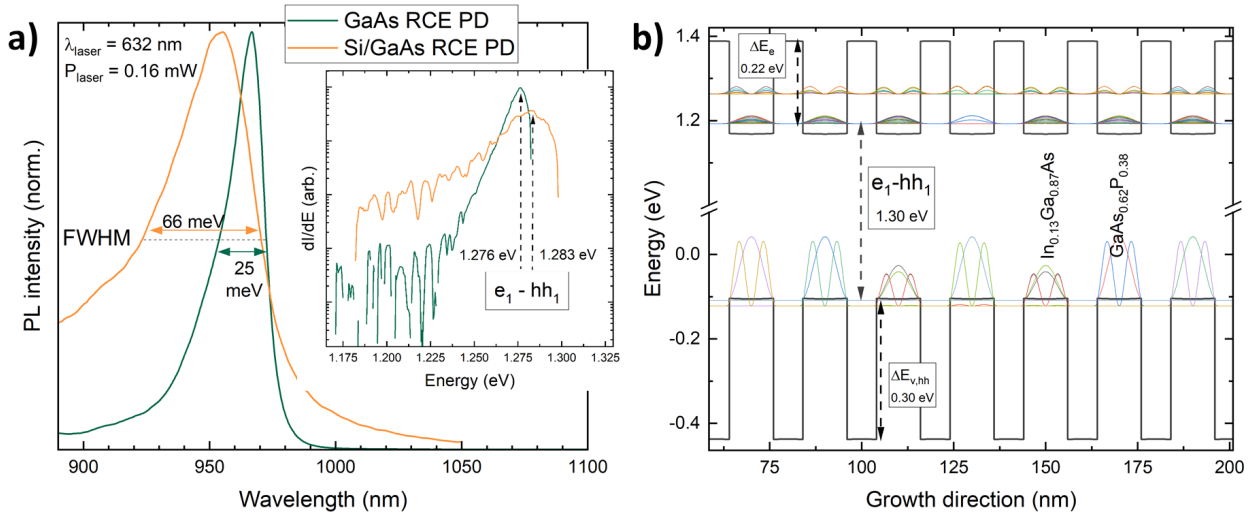


Figure 7: a) µ-photoluminescence spectra of the RCE PDs as well as their first-order derivatives (inset). b) The Schrödinger one-band model of the superlattice.

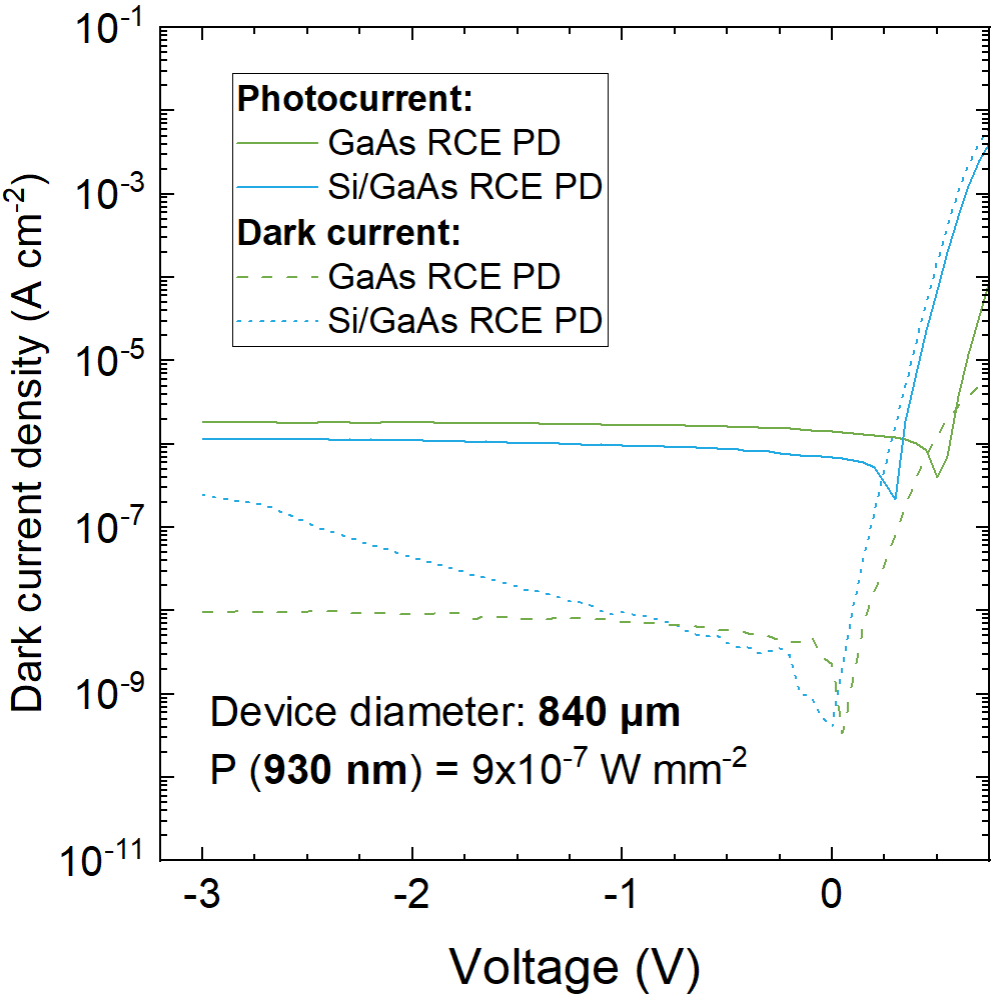


Figure 8: Dark current and photocurrent densities of the RCE PDs.

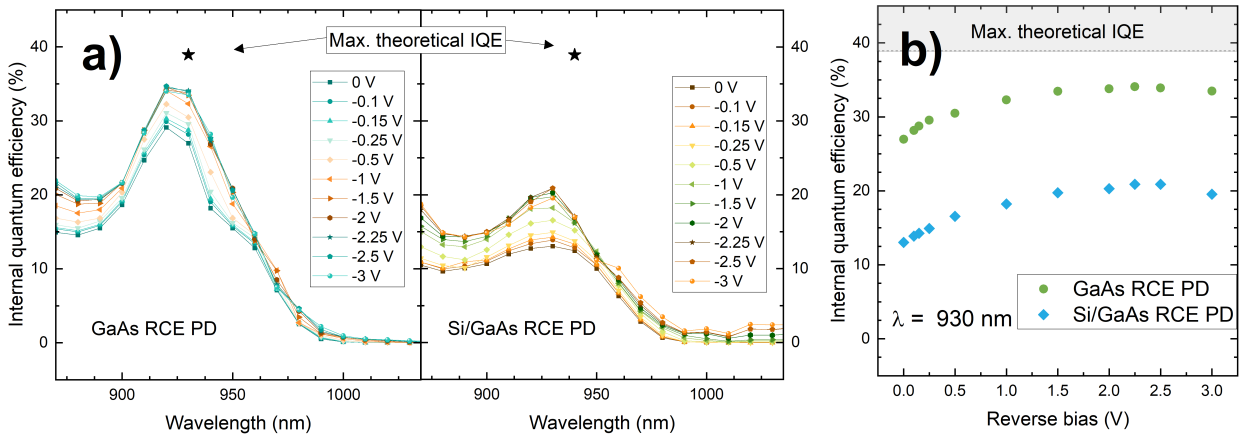


Figure 9: Internal quantum efficiency of the RCE PDs a) as a function of wavelength, and b) as a function of reverse bias at $\lambda = 930$ nm.