Cryogenic electronics for quantum computing ICs: what can bring FDSOI

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We present an overview of the performances of FDSOI CMOS transistors down to deep cryogenic temperature, highlighting in particular the benefits brought by the back bias. FDSOI transistors are operational from room temperature down to temperature as low as 100mK. The main DC electrical characteristics, as well as variability properties and reliability are measured and analyzed. We also point out specific behaviors appearing at cryogenic temperature, and discuss their physical origin and modeling.

Introduction

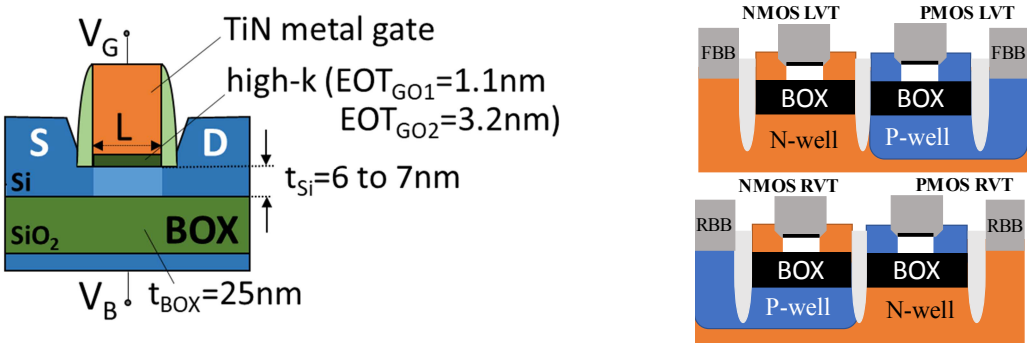
To design efficient quantum computers, conventional electronics is required as close as possible to the quantum bit (qubit) devices, considering either superconducting or Si-spin qubits, for the read-out and control, thus reducing the need for wiring toward room temperature (1). This need highlights the broad importance of exploring and developing low-temperature CMOS technologies, with operation temperatures ranging from 4.2K down to well below 1K. Moreover, the Si-spin qubit process is also compatible with the CMOS process, allowing both of them, in principle, to be monolithically integrated on a single chip (2),(3). This could provide an essential building block for any large-scale quantum processors, by enabling the design of scalable close-to-qubit cryogenic electronics for massive qubit matrix indexation and, ultimately, development of fault-tolerant universal gate-based quantum computers (4).

In this approach, FDSOI technologies appear as a valuable solution, with their unique property of being able to adjust its threshold voltage (V_{th}) as a function of the temperature by the mean of a back bias V_B. FDSOI thus enables high performance and low-power electronics. However, there is currently no process design kit to design CMOS circuits at cryogenic temperature, whatever the technology node considered. Therefore, extensive electrical characterization is required, with the aim of building a future cryogenic compact model, or at least of providing analytical and physics based models to designers in order to help them to optimize their circuits (5).

In this work, we present an overview of the performances of FDSOI CMOS technology down to deep cryogenic temperature, with specific attention to devices electrostatics, variability or thermal effects. Because these aspects are essential for the development of compact models and robust design tools, we present recent progresses in electrical characterization and analysis of FDSOI MOSFETs down to 100mK, and the underlying physics, highlighting the effect of the back bias V_B.

Electrical Performances

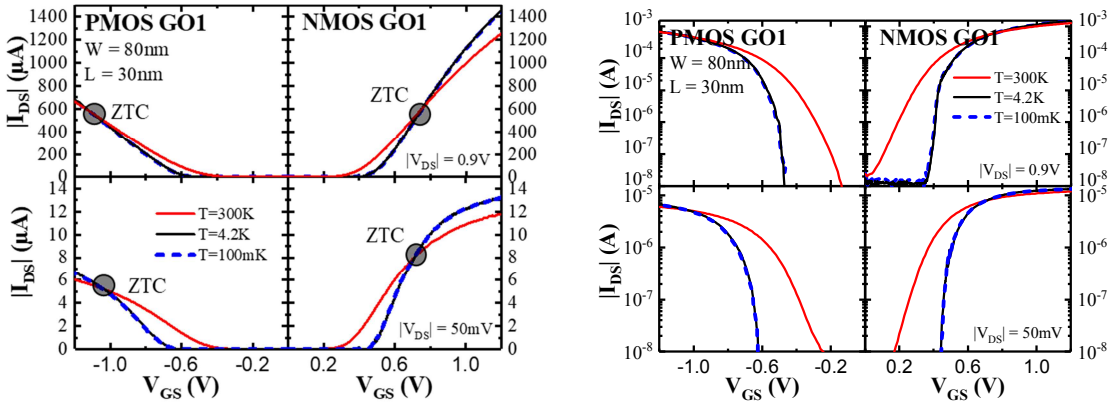
We summarize here the measurements performed on 28nm FDSOI transistors (see schematics in Fig.1) with a thin (GO1, EOT =1.1nm) and thick gate oxide (GO2, EOT=3.2nm) (6),(7). Regular-V_{TH} (RVT) and low-V_{TH} (LVT) transistors are obtained with a doped back plane below the BOX. This doped back plane allows in addition the biasing of the back interface in forward (FBB) and reverse (RBB) (8). NMOS and PMOS devices, with both V_{TH}-flavors, with GO1 and GO2, have been extensively characterized from room temperature down to 100mK.



(a) (b)

Figure 1. (a) Schematics of a FDSOI transistor studied here. (b) N- and PMOS 28nm FDSOI with regular (RVT) and low-VTH (LVT) flavors with N/PWELL ($N_{A,D}$~$10^{18}cm^{-3}$).

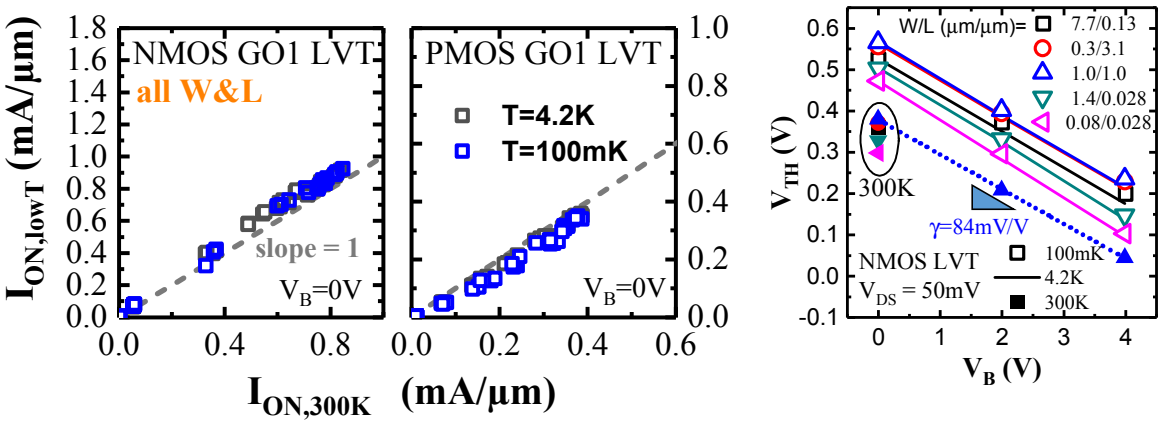
Lowering temperature is expected to drastically improve the main electrical characteristics of transistors, like the carrier mobility, due to the suppression of the phonon scattering contribution, and the subthreshold slope, which follows the Maxwell-Boltzmann limit in k_B.T (9).



(a) (b)

Figure 2. (a) I_{DS} measured as a function of V_{GS} for NMOS and PMOS GO1 at high and low V_{DS} ($|V_{DS}|$=0.9V and $|V_{DS}|$=50mV respectively) for T=300K, 4.2K and 100mK. A zero temperature variation point (ZTC) is evidenced for all devices, in linear and saturation regime. (a) Same plot as Fig.2a in log-scale to show the subthreshold region. Curves at 4.2K and 100mK are completely superimposed whatever V_{DS} or V_{GS} values.

We have shown that transistors can fully operate from room temperature down to 100mK, as illustrated in Fig.2. Both NMOS and PMOS exhibit an improved subthreshold slope and a higher drain current in either linear or saturation regime. However, we did not observe any significant differences between 4K and 100mK in any electrical characteristics (Fig.3a), suggesting that transport properties remains unchanged in this range of temperature, even in the subthreshold regime. More generally, no additional benefit is observed below 20K.



(a) (b)

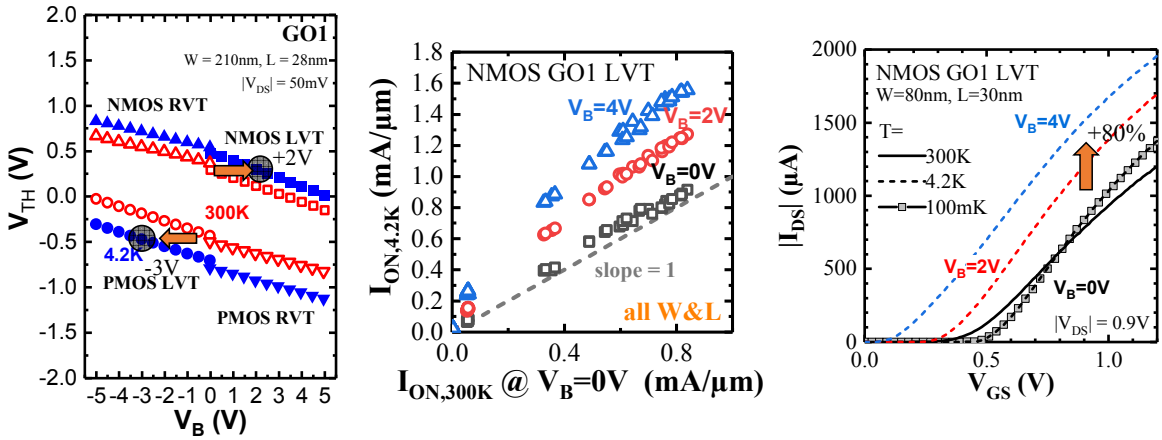
Figure 3. (a) Low temperature ON-current I_{ON} (@T=4.2K and T=100mK) measured at $|V_{GS}|=|V_{DS}|=0.9V$ on NMOS and PMOS GO1 transistors as a function of I_{ON} measured at 300K (W=80nm and 1µm, L varying from 25µm to 28nm). (b) V_{TH} measured as a function of V_B at different temperatures (300K, 4.2K and 100mK) on NMOS GO1 with various dimensions

Interestingly, in all the transfer characteristics (i.e. I_{DS} vs. V_{GS} curves) we can observe a Zero-Temperature-Coefficient point (ZTC), corresponding to a given voltage for which the drain current I_{DS} exhibits zero temperature dependence, *i.e.* $dI_{DS}/dT=0$. We notice that this ZTC point occurs around $V_{GS}=0.6V$ for NMOS GO1 and GO2, and above $|V_{GS}|=1V$ for PMOS GO1 and GO2, and slightly varies with V_{DS} and the transistor geometry (W and L). This ZTC point results from the temperature behavior of the Fermi–Dirac function, which controls the subband carrier population (10), and is not due to a compensation effect between carrier mobility and threshold voltage temperature variation as sometimes stated. This ZTC point is responsible in particular of the low I_{ON} improvement at $|V_{GS}|=0.9V$ for GO1 devices shown in Fig.3a.

In the following, we will see how the ability to apply a back bias can further improve the performances of transistors in cryogenic conditions.

Effect of the back bias V_B on electrical performances

Fig.3b shows the effect of V_B on the threshold voltage measured at 300K, 4.2K and 100mK: we see that the body factor delta=dV_{TH}/dV_B, which defines the efficiency of V_B to tune V_{TH}, is preserved down to 100mK despite the potential dopant freeze-out effect of the GP.



(a) (b) (c)

Figure 4. (a) Measured V_{TH} vs. V_B for N- and PMOS, RVT and LVT, GO1, at 300K and 4.2K ($|V_{DS}|$=50mV, W=80nm, L=28nm). (b) I_{ON} measured at 4.2K as a function of I_{ON} measured ar 300K for different FBB (V_B=0V, 2V and 4V) on NMOS LVT GO1 with different dimensions (W=80nm and 1µm, L varying from 25µm to 28nm). Only small I_{ON} gain is observed at V_B=0V due to ZTC. (c) Drain current I_{DS} measured as a function of V_{GS} on a NMOS LVT GO1 for different temperatures and V_B (L=28nm, 80nm).

One of the main drawback of operating transistors at low temperature, is the subsequent increase of the threshold voltage, by an amount of 0.6mV/K to 1mV/K depending on the MOS type and technology (11),(12). Consequently, V_{TH} can shift by more than 150mV at 4.2K (see Fig.4a). Using a FBB in the range of $|V_B|$=1V to 3V, depending on NMOS or PMOS type and of the gate oxide thickness GO1 or GO2, it is possible to shift the threshold voltage back to its value at RT, and so to reduce the power consumption.

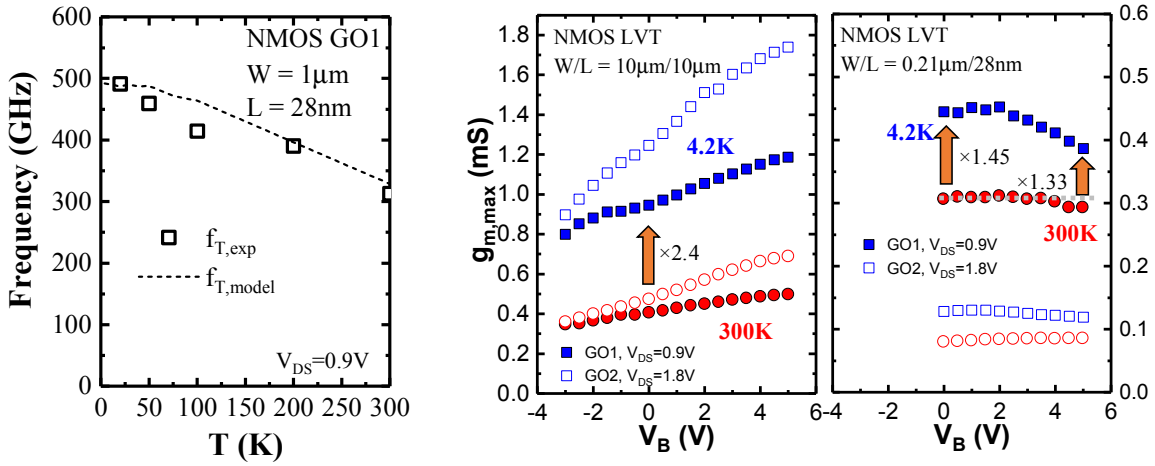
We have shown in the previous section that for V_B=0V the gain on I_{ON} is small, due to Zero Temperature Coefficient (ZTC) point in I_{DS}-V_{GS} curves for NMOS and PMOS ($|V_{ZTC}|$≈0.6V to 1V) which leads to a slight T-dependence of I_{ON}. By applying a FBB, it is possible to maintain the same overdrive at $|V_G|$=0.9V as at RT, and so to take benefits from the carrier mobility increase at a given carrier density – which is still roughly given by $C_{OX}\times|V_{GS}-V_{TH}|$ whatever the temperature –, thus overcoming the previously mentioned ZTC effect (Fig.4b and Fig.4c).

RF figure of merit improvement

DC measurements can also be used to estimate some RF figures of merit, like the current-gain cutoff frequency f_T, using for instance the following expression:

$$f_T = \frac{g_{m,max}}{2\pi C_{ox} WL} \qquad [1]$$

where C_{OX} is the gate oxide capacitance, and $g_{m,max}$ is the maximum of the transconductance. In Fig.5, we checked the good agreement between Eq.1 and RF measurements on the whole range of temperature down to 4.2K, considering C_{OX} is independent of temperature. For NMOS GO1 with L=28nm, we observed a gain in $g_{m,max}$ and so in f_T by ≈45% at 4.2K with respect to RT (Fig.5). Based on g_m measurements as a function of temperature and V_B, we see that, this gain decreases with FBB applied at 4.2K , but can be however kept as high as 33% for V_B=4V (Fig.5b).

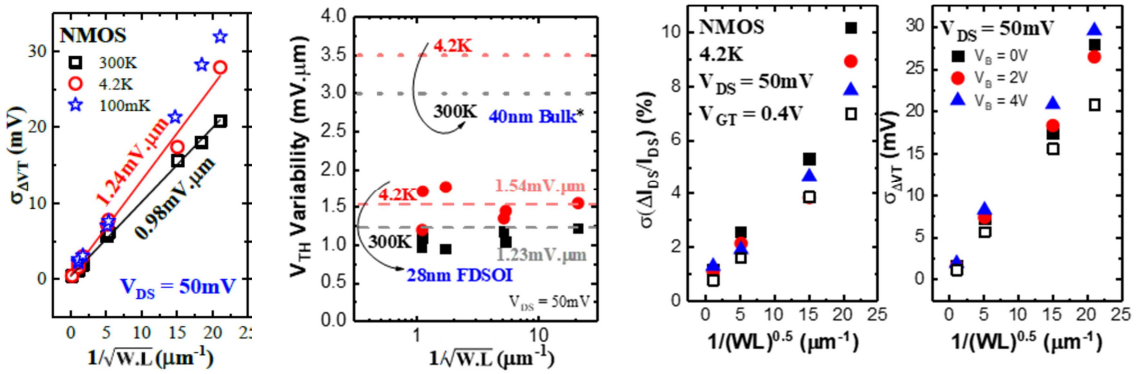


(a) (b)

Figure 5. (a) Cut-off frequency f_t measured as a function of temperature on a NMOS GO1 (symbols, L=28nm), and calculated f_t using the corresponding measured value of $g_{m,max}$ and Eq.1 (dotted line). (b) Maximum transconductance $g_{m,max}$ measured as a function of V_B at T=300K and T=4.2K on NMOS GO1 and GO2 (left, L=10µm, right, L=28nm).

Other electrical parameters: variability and reliability

Another advantage of FDSOI technology, is the better mismatch and variability properties compared to bulk technology offered by the undoped channel (13). Statistical analysis on variability and mismatch down to 100mK has been performed using an addressable matrix of transistors (14),(15), thus reaching a total of ≈3000 measured transistors. From the analysis performed over all transistor's dimensions and types, we concluded that the V_{TH} variability degrades as the operation temperature decreases, but

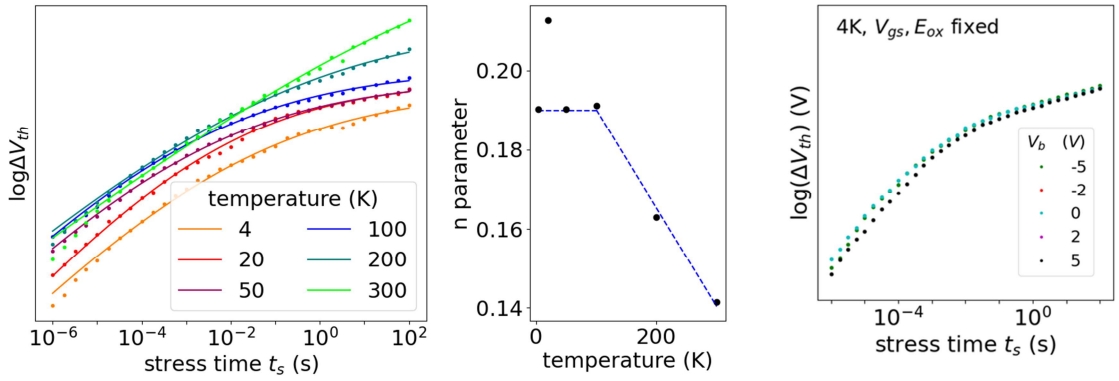


(a) (b) (c)

Figure 6. (a) Pelgrom plot of V_{TH} variability for NMOS (V_{DS}=50mV) at T=300K, 4.2K and 100mK. (b) $A_{\Delta VT}$ vs. $1/\sqrt{W.L}$ for NMOS, at V_{DS}=50mV, T=4.2 K and 300 K. Dashed lines indicate the extracted linear slope values from the Pelgrom plots. Dotted lines indicate 40nm bulk CMOS technology (23). (c) *left* - $\sigma(\Delta I_{DS}/I_{DS})$ vs. $1/\sqrt{W.L}$ measured on NMOS (V_{DS}=50mV and V_{GS}-V_{TH}=0.4V) varying V_B. *right*- corresponding $\sigma(\Delta V_T)$ vs. $1/\sqrt{W.L}$ (V_{DS}=50mV). FBB slightly reduces I_{DS} variability, without significant impact on V_{TH} variability.

this degradation is not dramatic. For instance at 4.2K, the individual matching parameter (iA_{VT}) of NMOS GO1 transistors increases from 0.98mV.µm at RT to 1.24mV.µm at 4.2K, which remains low (Fig.6). Such degradation has also been observed on other technologies with roughly the same extent (16),(17). This degradation at low temperature has been attributed to the impact of disorder-induced band tail states, with energies located close to the bottom of the conduction band and the top of the valence band (18),(19). Indeed, around $V_{TH,}$ the Fermi level of the channel probes these band tail states at low temperature leading to additional fluctuations of $V_{TH,}$ in correlation with the sub-threshold slope saturation (20),(21) or the excess 1/f noise (22). The effect of V_B on current and V_{TH} variability is illustrated in Fig.6c for a NMOS GO1 transistor at 4.2K. We see that the V_{TH} mismatch does not depend on V_B at 4.2K, as at RT (13). On the other hand, a FBB can help reduce the drain current variability, especially at high V_{GT}.

Bias temperature instabilities (BTI) is one of the mechanism which can limit the reliability of transistors. BTI degradation is generally described by a thermally activated model, so that the V_{TH} shift due BTI is expected to decrease with T, and disappear at sufficiently low temperature. Ultra-fast BTI measurements have been performed on NMOS and PMOS devices at cryogenic temperature down to 4.2K (24).



(a) (b) (c)

Figure 7. (a) Measured shift in the threshold voltage during PBTI stress (ΔV_{TH}) as a function of stress time (symbols), and corresponding curves fitted with a classical stress model (see Eq.2). (b) Evolution of the parameter *n* with T of the classical model. (c) Shift in the threshold voltage during PBTI stress measured at 4K at different V_B at constant oxide field E_{OX}.

We identified two regimes of temperature dependence for the time acceleration parameter *n* describing the evolution of the V_{TH} shift, due to a PBTI stress, with stress time t_s and stress voltage $V_{GS,stress}$ following the classical model:

$$\Delta V_{TH}(t_s, V_{GS,stress}) \propto \frac{1}{1+At_s^{-n}V_{GS,stress}^{\gamma}} \quad [2]$$

From 300K down to 100K, n varies linearly with T; below 100K, *n* saturates, indicating a change in the dominant physical mechanism responsible for the PBTI degradations. At room temperature, the degradation is mostly due to a thermally activated phenomenon (a non-radiative multi-phonon process). On the contrary, at low temperature the dominant source of degradation does not depend on temperature anymore, as is the case for elastic tunneling of carriers from the channel to traps in the gate oxide. Similar results have been observed for bulk CMOS NMOS transistors(16), confirming the remaining of a temperature-independent trapping mechanisms that dominates below

100K. To go further, we evaluated the effect of a back bias on PBTI degradation (Fig.7c). We did not observe any significant dependence with V_B at 4.2K, for V_B ranging from -5V to +5V. Therefore, back bias can be an efficient knob to mitigate BTI stress by reducing the gate voltage used to operate transistors without additional degradation induced by V_B.

Overall perfomances at low temperature

TABLE I. Benchmark of NMOS performances at 300K and 4.2K: 28nm FDSOI (this work) vs. 40nm (23) & 28nm Bulk CMOS (16).

		This work 28nm FDSOI L = 28nm		40nm Bulk L = 40nm		28nm Bulk L = 28nm	
		300K	4.2K	300K	4.2K	300K	4.2K
V_{TH} (V)	V_B=0V	0.29	0.49			0.31	**0.41**
	V_B=2V		**0.29**				
I_{ON}/W (µA/µm)	V_B=0V	689	790	442	**500**	694	**893**
	V_B=2V		**1088**				
I_{OFF}/W (pA/µm)	V_B=0V	900	<0.01*				
	V_B=2V		**<0.01***				
SS (mV/dec) @ V_{DD}		74	**4.8**	88	**28**	89	**20**
Weak inversion:							
g_m/I_{DS} (V^{-1})		31.2	**300**	27	**92**		
A_V (V/V)		27	**36**	20.8	**23**		
A_{VT} (mV.µm)		0.98	**1.24**	3.0	**3.5**	1.85	**2.02**
$A_{\Delta\beta/\beta}$ (%.µm)		0.51	**0.74**	0.46	**0.91**		

Table I summarizes the evolution of the overall performances of FDSOI transistors when temperature is decreased from RT to 4.2K. The back bias ability clearly brings an advantage over bulk technologies to improve and optimize LT operation of transistors, and more generally of circuits, like demonstrated for instance on ring oscillators (25) or a transimpedance amplifier (3).

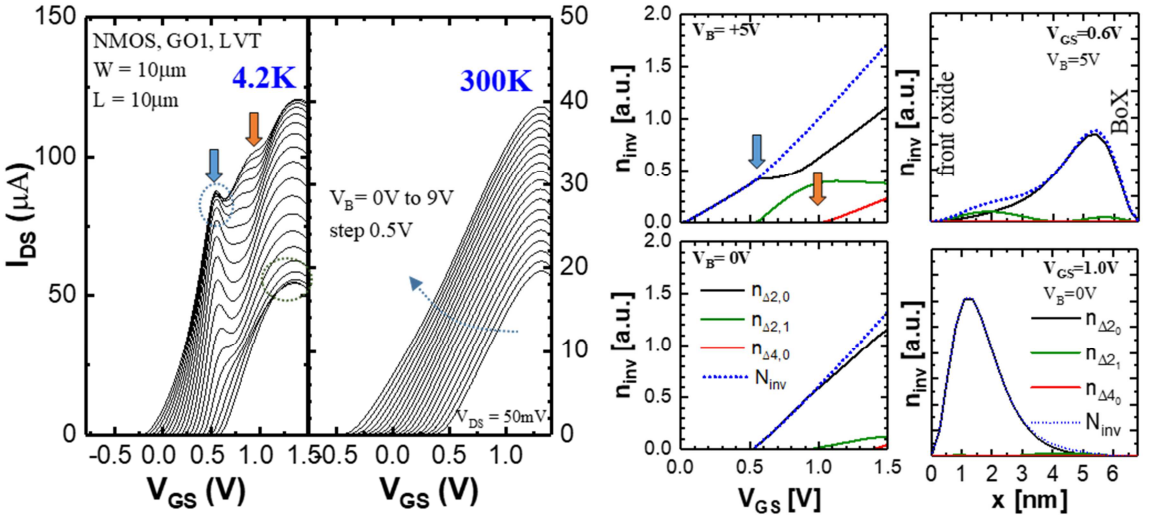
Transistor modeling

Modeling issues are addressed in this part. Besides serious numerical difficulties due to singularities appearing at low temperature when solving model equations (5), the change of important physical parameters (like carrier mobility, thermal conductivity,…) needs to be correctly taken into account in future compact or analytical models. In addition, new physical effects evidenced at low temperature also need to be understood, analytically modeled and included as well.

Effect of back bias on the electrostatics and transport properties of the FDSOI transistors

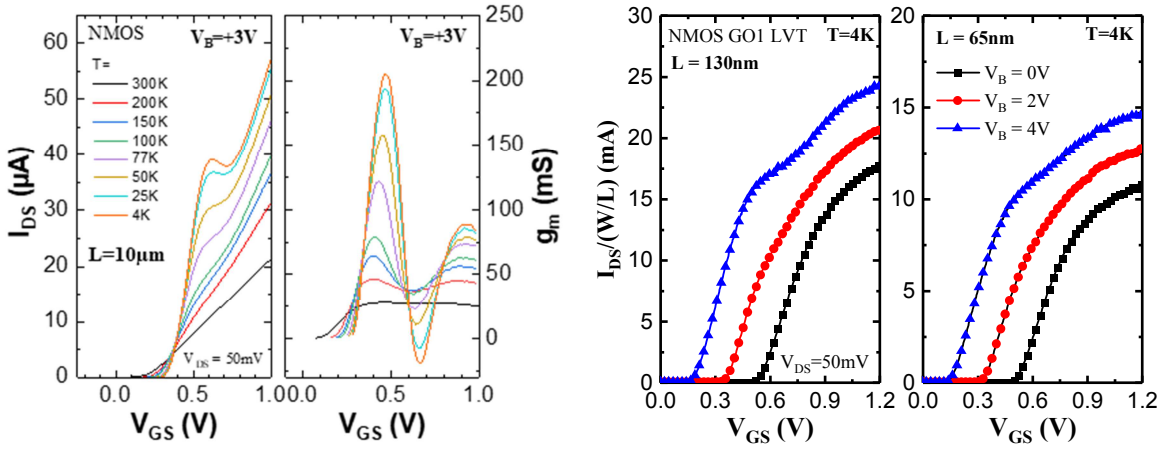
We have evidenced that V_B modifies the transfer characteristic I_{DS} vs. V_{GS} of NMOS GO1 and GO2, especially for long channel transistors, as illustrated in Figs.8&9. At low temperature (typically for T<100K), when VB is biased in FBB, the drain current exhibits humps in I_{DS}, at given values of V_{GS}. These values correspond exactly to the voltage bias for which a new energy subband becomes populated by electrons (Fig.8). As a consequence, intersubband scattering (IS) can occur, and the electron mobility suddenly drops (26). This is a specific feature arising at low temperature, and associated with thin film devices (27). This effect, which becomes observable at T<100K, can be mitigated on

shorter L (Fig9b) – due to ballistic transport – and at high V_{DS} (28). Intersubband scattering could not been evidenced on our PMOS, which could be explained by the lower effective mass of holes in Si. On the transconductance curves g_m vs. V_{GS}, these humps leads to oscillations, with negative values of g_m (Fig.9a).



(a) (b)

Figure 8. (a) I_{DS} vs. V_{GS} measured on a long NMOS GO1 transistor at T=4.2K and T=300K. and for different FBB values from 0V to 9V. At 4.2K and in FBB, I_{DS} exhibits two humps around V_{GS}=0.54V and V_{GS}=0.9V indicated by the arrows. (b) Inversion carrier density calculated using 2D-Poisson Schrödinger solver as a function of V_{GS}, for V_B=+5V (top left) and V_B=0V (bottom left), for the first three lowest energy subbands, and inversion carrier density distribution as a function of position *x* in the channel for two given values of V_{GS} and V_B (right). The arrows indicate the onset of the second and third energy subband.



(a) (b)

Figure 9. (a) I_{DS} measured as function of V_{GS} (left) and corresponding transconductance gm vs. V_{GS} (right) on a long NMOS GO1 transistor (L=10µm), for V_B=3V, and for different temperatures from 300K down to 4K. (b) I_{DS} vs. V_{GS} measured at T=4K on NMOS transistors with L=130nm (left) and L=65nm (right), for different V_B, showing attenuation of the IS effect.

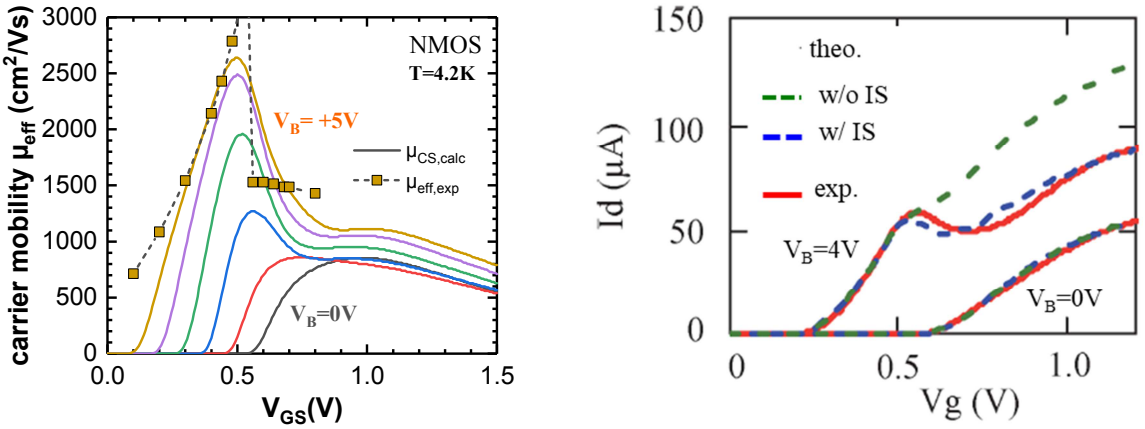
A look at the inversion carrier density across the Si channel reveals that IS effect occurs when the front channel is opening whereas back channel was already open, and reciprocally (7) (see Fig.8b). Although the theoretical model describing intersubband scattering is known (26),(29), phenomenological equations can be used to have a more analytical model (30). In this simplified approach, front and back channel mobility can be evaluated separately at each interface with:

$$\mu_{\mathrm{eff},tot} = \frac{\mu_{\mathrm{eff}_1} N_{inv_1} + \mu_{\mathrm{eff}_2} N_{inv_2}}{N_{inv_1} + N_{inv_2}} \qquad [3]$$

in which 1 and 2 indexes stand for front channel and back channel. Intersubband scattering can be taken into account when $E_F > E_i$, where E_i corresponds to the second or third subband energy level, through an additional explicit dependence of the mobility at one interface with the inversion charge density at the other interface of the form:

$$\mu_{\mathrm{eff}_{2,\mathrm{IS}}} = \mu_{\mathrm{eff}_2}\left[a + b.exp\left(-\frac{N_{inv_1}}{c}\right)\right] \qquad [4]$$

in which *a, b* and *c* are fitting parameters,.



(a) (b)

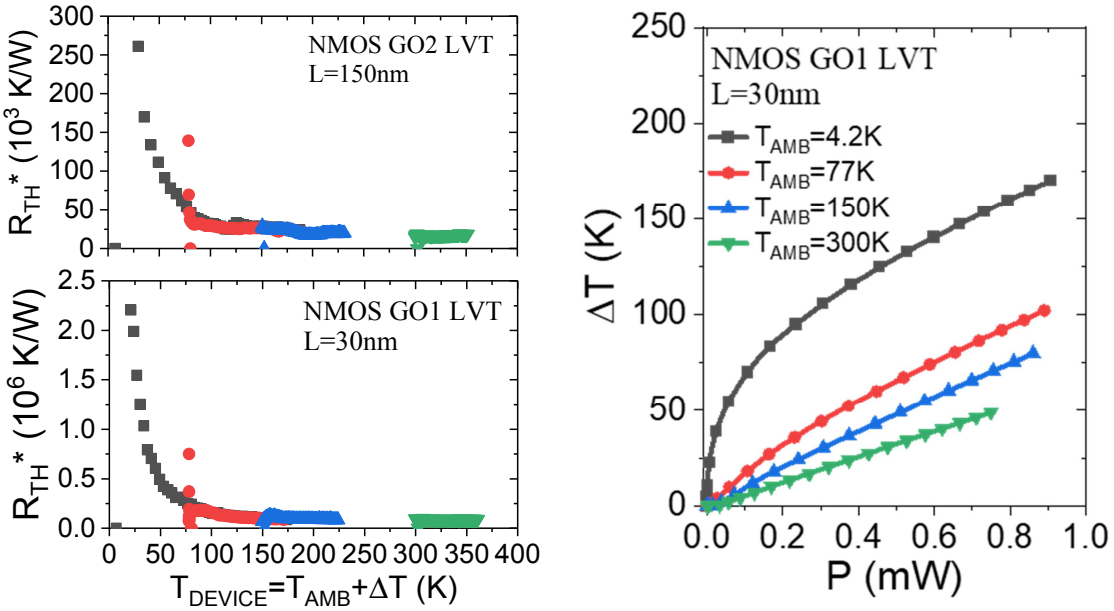
Figure 10. (a) Electron mobility extracted as a function of V_{GS} for different V_B (line), and calculated mobility with intersubband scattering at V_B=5V (symbols). (b) Drain current vs. front gate voltage Vg: Experimental (red solid line) and modeled with IS (dashed blue line) and modeled without IS (green dashed line) for V_B = 4 V and 0 V at T = 4.2 K.

Finally, Lambert-W function enables to accurately model the inversion charge and drain current from weak to strong inversion regime. We have shown that it remains valid down to ultra-low temperature, and can thus be applied for parameter extraction at low T (31).

Thermal effects and differential thermal resistance

Thermal effects play a fundamental role in cryogenic electronics, for which circuits are targeted to operate at various temperature stages, with limited cooling power. The study of self-heating effects at cryogenic temperature in this regard provides valuable information on how to manage thermal effects. It is also important for reliability, as it increases hot carrier degradation (32). To describe thermal effects, we extracted the differential thermal resistance defined as $R_{th}^{*}=d\Delta T/dP$ (33), where ΔT is the temperature increase in the channel of the transistor due to self-heating effect, and $P=I_{DS}\times V_{DS}$ is the

input power. Measurements have been performed using the gate thermometry method on transistors with two-contacts gate. Our results show that R_{th}^* is strongly temperature dependent as illustrated in Fig.11a, mainly due to the temperature dependence of the Si and SiO_2 thermal conductivity. However, we have evidenced a strong increase of R_{th}^* below T≈75K by several order of magnitude on all our devices. This huge thermal resistance at very low temperature leads to a strong non-linearity of ΔT with P, contrary to what is usually observed at room temperature (Fig.11b). The temperature of the channel measured by the gate resistance can be extracted as a function of gate voltage V_{GS}, revealing high temperature increase with respect to the ambient temperature T_{amb}=4.2K, up to 100K (7). The channel temperature in cryogenic environment can thus highly differ from the ambient temperature. This temperature increase needs to be taken into account when analyzing electrical parameters at low temperature, in particular when considering the saturation velocity or to extract the correct temperature dependence of the drain current.



(a) (b)

Figure 11. (a) Differential thermal resistance R_{TH}^* vs. $T_{dev}=T_{amb}+\Delta T$ extracted by the gate resistance method on NMOS GO1 (bottom, L=30nm) and NMOS GO2 (top, L=150nm) showing a strongly T-dependent behavior, with a high increase below T=75K. (b) ΔT increase in the channel extracted as a function of input power for different ambient temperatures from 300K down to 4K.

Conclusions

We gave an overview of the extensive electrical characterization performed on 28nm FDSOI transistors down to ultra-low temperature. New physical effects arising at low temperature have been investigated and discussed, highlighting specific issues to be addressed in a future DC and RF cryogenic compact model. However, ways of optimization already exists, using the unique opportunity offered by the back bias in FDSOI technology.

Acknowledgments

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References

1. E. Charbon et al., *IEEE Int. Electron Devices Meet.*, 343–346 (2016).
2. P. Galy et al., *IEEE J. Electron Devices Soc.*, **6**, 594–600 (2018).
3. L. Le Guevel et al., *Appl. Phys. Rev.*, **7** (2020).
4. X. Xue et al., *Nature*, **593**, 205–210 (2021).
5. C. Enz, A. Beckers, and F. Jazaeri, in *IEEE International Electron Devices Meeting (IEDM)*,, p. 529–532 (2020).
6. N. Planes et al., in *Symposium on VLSI Technology, Digest of Technical Papers*, vol. 33, p. 133–134 (2012).
7. M. Cassé et al., in *IEEE International Electron Devices Meeting (IEDM)*, p. 827–830 (2022).
8. J.-P. Noel et al., *IEEE Trans. Electron Devices*, **58**, 2473–2482 (2011).
9. F. Balestra and G. Ghibaudo, *Device and Circuit Cryogenic Operation for Low Temperature Electronics*, Springer, (2001).
10. E. Catapano, T. M. Frutuoso, M. Casse, and G. Ghibaudo, *IEEE Trans. Electron Devices*, **70**, 845–849 (2022).
11. A. Beckers, F. Jazaeri, and C. Enz, in *Proceedings of European Solid-State Device Research Conference*, p. 94–97 (2019).
12. W. Chakraborty et al., *IEEE J. Explor. Solid-State Comput. Devices Circuits*, **7**, 184–192 (2021).
13. F. Andrieu et al., in *Symposium on VLSI Technology, Digest of Technical Papers*, p. 57–58 (2010).
14. B. Cardoso Paz et al., in *IEEE International Conference on Microelectronic Test Structures*,, p. 8–12 (2020).
15. B. Cardoso Paz et al., in *Symposium on VLSI Technology, Digest of Technical Papers*, p. TN2.1 (2020).
16. A. Grill et al., *IEEE Int. Reliab. Phys. Symp. Proc.*, 7–8 (2020).
17. P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, *IEEE J. Electron Devices Soc.*, **8**, 263–273 (2020).
18. E. Arnold, *Appl. Phys. Lett.*, **25**, 705–707 (1974).
19. Y. Pan and M. Kleefstra, *Semicond. Sci. Technol.*, **5**, 312–318 (1990).
20. G. Ghibaudo et al., *Solid. State. Electron.*, **170**, 107820 (2020).
21. H. Bohuslavskyi et al., *IEEE Electron Device Lett.*, **40**, 784–787 (2019).
22. R. Asanovski et al., in *IEEE International Electron Devices Meeting (IEDM)*, p. 712–714 (2022).
23. P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, *Proc. Eur. Solid-State Device Res. Conf.*, 98–101 (2019).
24. L. Contamin et al., *IEEE Int. Reliab. Phys. Symp. Proc.*, 31–36 (2022).
25. L. Le Guevel et al., in *IEEE International Solid- State Circuits Conference (ISSCC)*, (2020).

26. M. Cassé et al., *Appl. Phys. Lett.*, **116**, 243502 (2020).
27. H.-C. Han et al., *Solid. State. Electron.*, **193**, 108296 (2022).
28. M. Casse et al., *IEEE Trans. Electron Devices*, **67**, 4636–4640 (2020).
29. S. Mori and T. Ando, *Phys. Rev. B*, **19**, 6433–6441 (1979).
30. M. Cassé and G. Ghibaudo, in *Low-Temperature Technologies and Applications*,, IntechOpen (2022).
31. F. Serra di Santa Maria et al., *Solid. State. Electron.*, **186**, 108175 (2021).
32. C. Prasad, *IEEE Trans. Electron Devices*, **66**, 4546–4555 (2019).
33. K. Triantopoulos et al., *IEEE Trans. Electron Devices*, **66** (2019).