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# Cryogenic Electronics For Quantum Computing ICs: What Can Bring FDSOI

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We present an overview of the performances of FDSOI CMOS transistors down to deep cryogenic temperature, highlighting in particular the benefits brought by the back bias. FDSOI transistors are operational from room temperature down to temperature as low as 100mK. The main DC electrical characteristics, as well as variability properties and reliability are measured and analyzed. We also point out specific behaviors appearing at cryogenic temperature, and discuss their physical origin and modeling.

## Introduction

To design efficient quantum computers, conventional electronics is required as close as possible to the quantum bit (qubit) devices, considering either superconducting or Si-spin qubits, for the read-out and control, thus reducing the need for wiring toward room temperature (1). This need highlights the broad importance of exploring and developing low-temperature CMOS technologies, with operation temperatures ranging from 4.2K down to well below 1K. Moreover, the Si-spin qubit process is also compatible with the CMOS process, allowing both of them, in principle, to be monolithically integrated on a single chip (2),(3). This could provide an essential building block for any large-scale quantum processors, by enabling the design of scalable close-to-qubit cryogenic electronics for massive qubit matrix indexation and, ultimately, development of fault-tolerant universal gate-based quantum computers (4).

In this approach, FDSOI technologies appear as a valuable solution, with their unique property of being able to adjust its threshold voltage ( $V_{th}$ ) as a function of the temperature by the mean of a back bias  $V_B$ . FDSOI thus enables high performance and low-power electronics. However, there is currently no process design kit to design CMOS circuits at cryogenic temperature, whatever the technology node considered. Therefore, extensive electrical characterization is required, with the aim of building a future cryogenic compact model, or at least of providing analytical and physics based models to designers in order to help them to optimize their circuits (5).

In this work, we present an overview of the performances of FDSOI CMOS technology down to deep cryogenic temperature, with specific attention to devices electrostatics, variability or thermal effects. Because these aspects are essential for the development of compact models and robust design tools, we present recent progresses in electrical characterization and analysis of FDSOI MOSFETs down to 100mK, and the underlying physics, highlighting the effect of the back bias  $V_B$ .

## Electrical Performances

We summarize here the measurements performed on 28nm FDSOI transistors (see schematics in Fig.1) with a thin (GO1, EOT =1.1nm) and thick gate oxide (GO2, EOT=3.2nm) (6),(7). Regular- $V_{TH}$  (RVT) and low- $V_{TH}$  (LVT) transistors are obtained with a doped back plane below the BOX. This doped back plane allows in addition the biasing of the back interface in forward (FBB) and reverse (RBB) (8). NMOS and PMOS devices, with both  $V_{TH}$ -flavors, with GO1 and GO2, have been extensively characterized from room temperature down to 100mK.

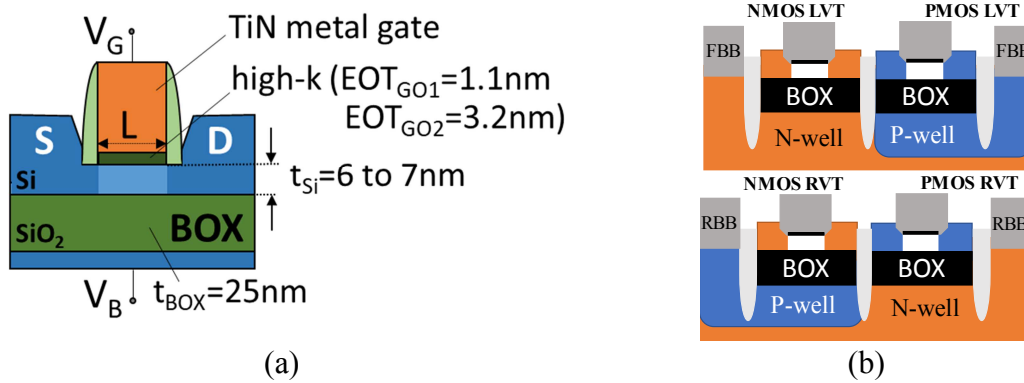


Figure 1. (a) Schematics of a FDSOI transistor studied here. (b) N- and PMOS 28nm FDSOI with regular (RVT) and low- $V_{TH}$  (LVT) flavors with N/PWELL ( $N_{A,D} \sim 10^{18} \text{cm}^{-3}$ ).

Lowering temperature is expected to drastically improve the main electrical characteristics of transistors, like the carrier mobility, due to the suppression of the phonon scattering contribution, and the subthreshold slope, which follows the Maxwell-Boltzmann limit in  $k_B \cdot T$  (9).

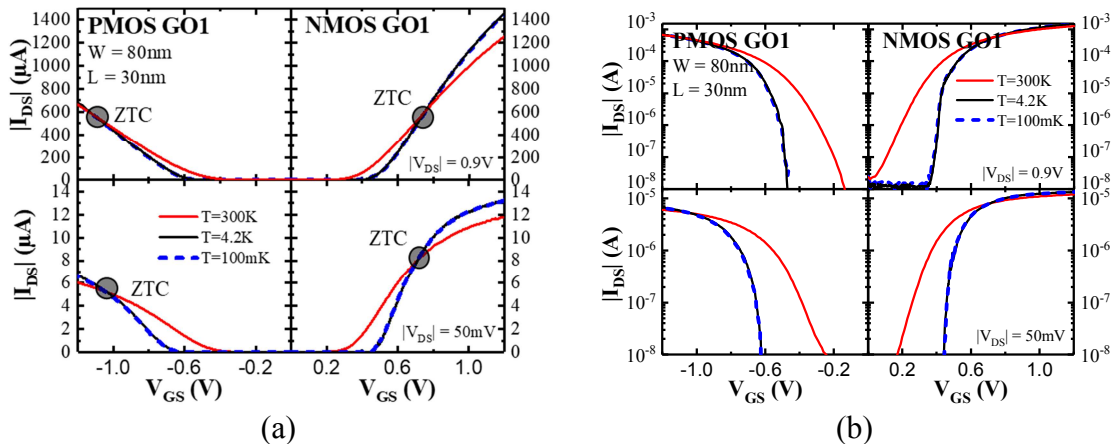


Figure 2. (a)  $I_{DS}$  measured as a function of  $V_{GS}$  for NMOS and PMOS GO1 at high and low  $V_{DS}$  ( $|V_{DS}|=0.9V$  and  $|V_{DS}|=50mV$  respectively) for  $T=300K$ ,  $4.2K$  and  $100mK$ . A zero temperature variation point (ZTC) is evidenced for all devices, in linear and saturation regime. (a) Same plot as Fig.2a in log-scale to show the subthreshold region. Curves at  $4.2K$  and  $100mK$  are completely superimposed whatever  $V_{DS}$  or  $V_{GS}$  values.

We have shown that transistors can fully operate from room temperature down to 100mK, as illustrated in Fig.2. Both NMOS and PMOS exhibit an improved subthreshold slope and a higher drain current in either linear or saturation regime. However, we did not observe any significant differences between 4K and 100mK in any electrical characteristics (Fig.3a), suggesting that transport properties remains unchanged in this range of temperature, even in the subthreshold regime. More generally, no additional benefit is observed below 20K.

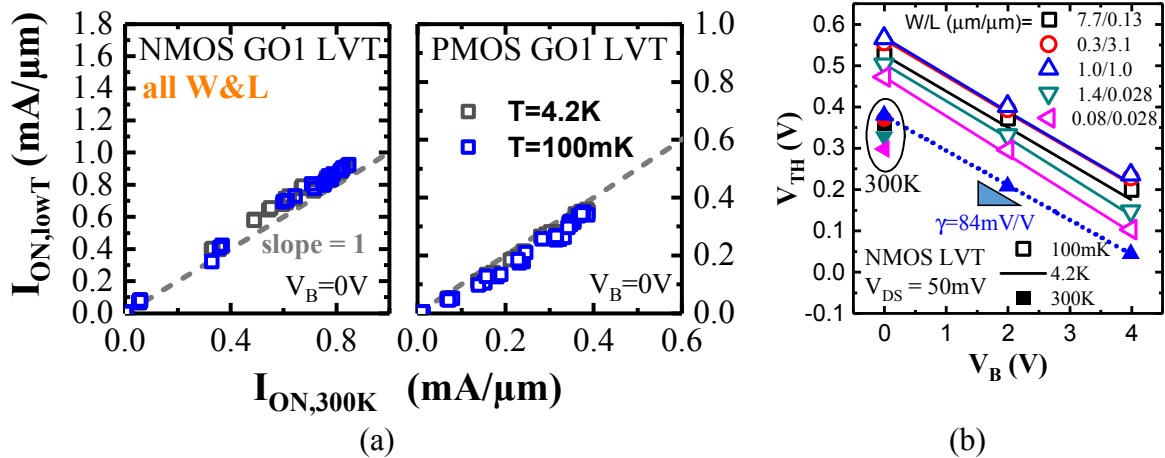


Figure 3. (a) Low temperature ON-current  $I_{ON}$  (@ $T=4.2\text{K}$  and  $T=100\text{mK}$ ) measured at  $|V_{GS}|=|V_{DS}|=0.9\text{V}$  on NMOS and PMOS GO1 transistors as a function of  $I_{ON}$  measured at 300K ( $W=80\text{nm}$  and  $1\mu\text{m}$ ,  $L$  varying from  $25\mu\text{m}$  to  $28\text{nm}$ ). (b)  $V_{TH}$  measured as a function of  $V_B$  at different temperatures (300K, 4.2K and 100mK) on NMOS GO1 with various dimensions

Interestingly, in all the transfer characteristics (i.e.  $I_{DS}$  vs.  $V_{GS}$  curves) we can observe a Zero-Temperature-Coefficient point (ZTC), corresponding to a given voltage for which the drain current  $I_{DS}$  exhibits zero temperature dependence, i.e.  $dI_{DS}/dT=0$ . We notice that this ZTC point occurs around  $V_{GS}=0.6\text{V}$  for NMOS GO1 and GO2, and above  $|V_{GS}|=1\text{V}$  for PMOS GO1 and GO2, and slightly varies with  $V_{DS}$  and the transistor geometry ( $W$  and  $L$ ). This ZTC point results from the temperature behavior of the Fermi–Dirac function, which controls the subband carrier population (10), and is not due to a compensation effect between carrier mobility and threshold voltage temperature variation as sometimes stated. This ZTC point is responsible in particular of the low  $I_{ON}$  improvement at  $|V_{GS}|=0.9\text{V}$  for GO1 devices shown in Fig.3a.

In the following, we will see how the ability to apply a back bias can further improve the performances of transistors in cryogenic conditions.

#### Effect of the back bias $V_B$ on electrical performances

Fig.3b shows the effect of  $V_B$  on the threshold voltage measured at 300K, 4.2K and 100mK: we see that the body factor  $\delta=dV_{TH}/dV_B$ , which defines the efficiency of  $V_B$  to tune  $V_{TH}$ , is preserved down to 100mK despite the potential dopant freeze-out effect of the GP.

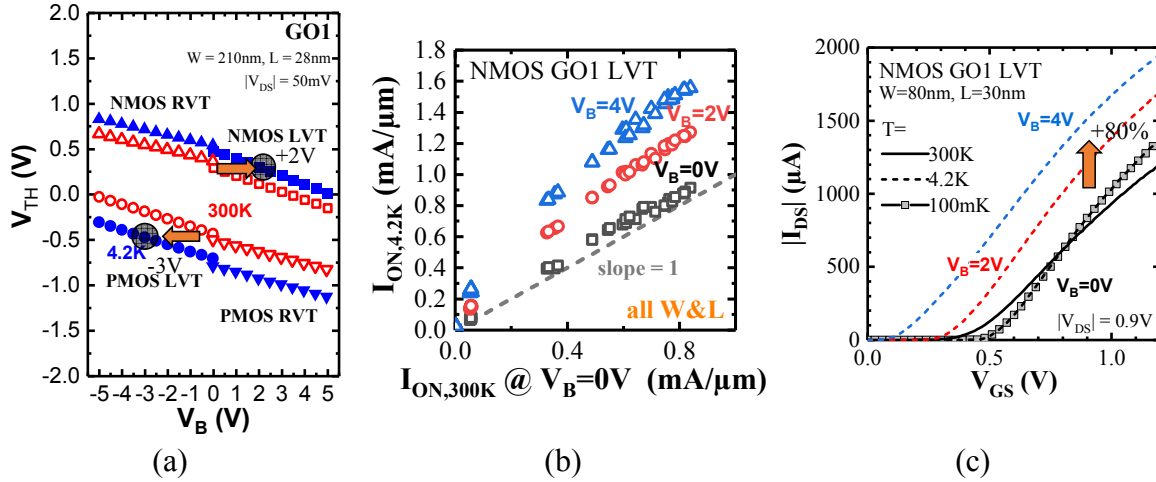


Figure 4. (a) Measured  $V_{TH}$  vs.  $V_B$  for N- and PMOS, RVT and LVT, GO1, at 300K and 4.2K ( $|V_{DS}| = 50mV$ ,  $W = 80nm$ ,  $L = 28nm$ ). (b)  $I_{ON}$  measured at 4.2K as a function of  $I_{ON}$  measured at 300K for different FBB ( $V_B = 0V, 2V$  and  $4V$ ) on NMOS LVT GO1 with different dimensions ( $W = 80nm$  and  $1\mu m$ ,  $L$  varying from  $25\mu m$  to  $28nm$ ). Only small  $I_{ON}$  gain is observed at  $V_B = 0V$  due to ZTC. (c) Drain current  $I_{DS}$  measured as a function of  $V_{GS}$  on a NMOS LVT GO1 for different temperatures and  $V_B$  ( $L = 28nm$ ,  $80nm$ ).

One of the main drawback of operating transistors at low temperature, is the subsequent increase of the threshold voltage, by an amount of  $0.6mV/K$  to  $1mV/K$  depending on the MOS type and technology (11),(12). Consequently,  $V_{TH}$  can shift by more than  $150mV$  at 4.2K (see Fig.4a). Using a FBB in the range of  $|V_B| = 1V$  to  $3V$ , depending on NMOS or PMOS type and of the gate oxide thickness GO1 or GO2, it is possible to shift the threshold voltage back to its value at RT, and so to reduce the power consumption.

We have shown in the previous section that for  $V_B = 0V$  the gain on  $I_{ON}$  is small, due to Zero Temperature Coefficient (ZTC) point in  $I_{DS} - V_{GS}$  curves for NMOS and PMOS ( $|V_{ZTC}| \approx 0.6V$  to  $1V$ ) which leads to a slight T-dependence of  $I_{ON}$ . By applying a FBB, it is possible to maintain the same overdrive at  $|V_G| = 0.9V$  as at RT, and so to take benefits from the carrier mobility increase at a given carrier density – which is still roughly given by  $C_{OX} \times |V_{GS} - V_{TH}|$  whatever the temperature –, thus overcoming the previously mentioned ZTC effect (Fig.4b and Fig.4c).

#### RF figure of merit improvement

DC measurements can also be used to estimate some RF figures of merit, like the current-gain cutoff frequency  $f_T$ , using for instance the following expression:

$$f_T = \frac{g_{m,max}}{2\pi C_{OX}WL} \quad [1]$$

where  $C_{OX}$  is the gate oxide capacitance, and  $g_{m,max}$  is the maximum of the transconductance. In Fig.5, we checked the good agreement between Eq.1 and RF measurements on the whole range of temperature down to 4.2K, considering  $C_{OX}$  is independent of temperature. For NMOS GO1 with  $L = 28nm$ , we observed a gain in  $g_{m,max}$  and so in  $f_T$  by  $\approx 45\%$  at 4.2K with respect to RT (Fig.5). Based on  $g_m$  measurements as a function of temperature and  $V_B$ , we see that, this gain decreases with FBB applied at 4.2K, but can be however kept as high as 33% for  $V_B = 4V$  (Fig.5b).

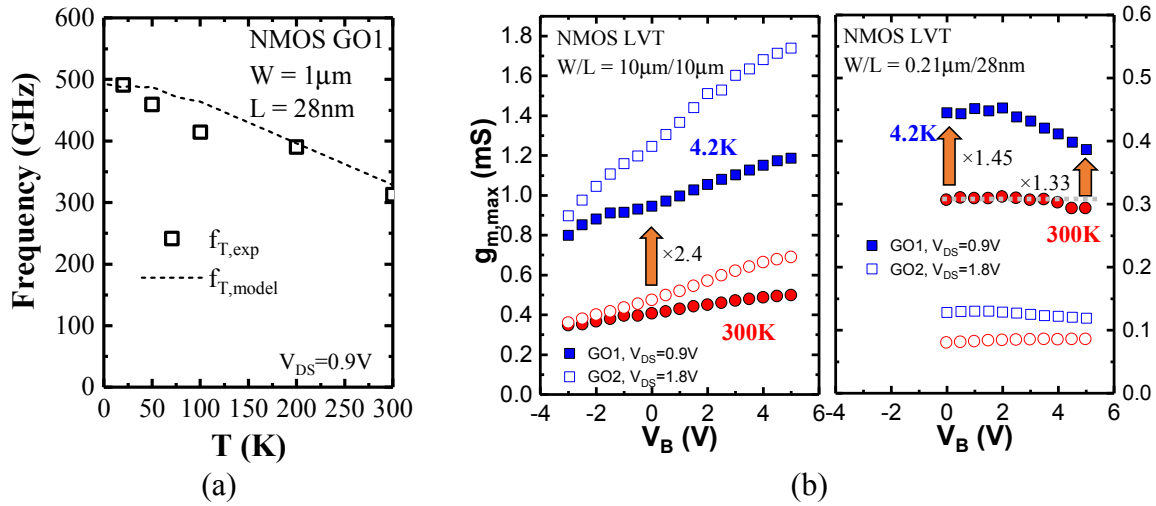


Figure 5. (a) Cut-off frequency  $f_t$  measured as a function of temperature on a NMOS GO1 (symbols,  $L=28\text{nm}$ ), and calculated  $f_t$  using the corresponding measured value of  $g_{m,\text{max}}$  and Eq.1 (dotted line). (b) Maximum transconductance  $g_{m,\text{max}}$  measured as a function of  $V_B$  at  $T=300\text{K}$  and  $T=4.2\text{K}$  on NMOS GO1 and GO2 (left,  $L=10\mu\text{m}$ , right,  $L=28\text{nm}$ ).

#### Other electrical parameters: variability and reliability

Another advantage of FDSOI technology, is the better mismatch and variability properties compared to bulk technology offered by the undoped channel (13). Statistical analysis on variability and mismatch down to 100mK has been performed using an addressable matrix of transistors (14),(15), thus reaching a total of  $\approx 3000$  measured transistors. From the analysis performed over all transistor's dimensions and types, we concluded that the  $V_{\text{TH}}$  variability degrades as the operation temperature decreases, but

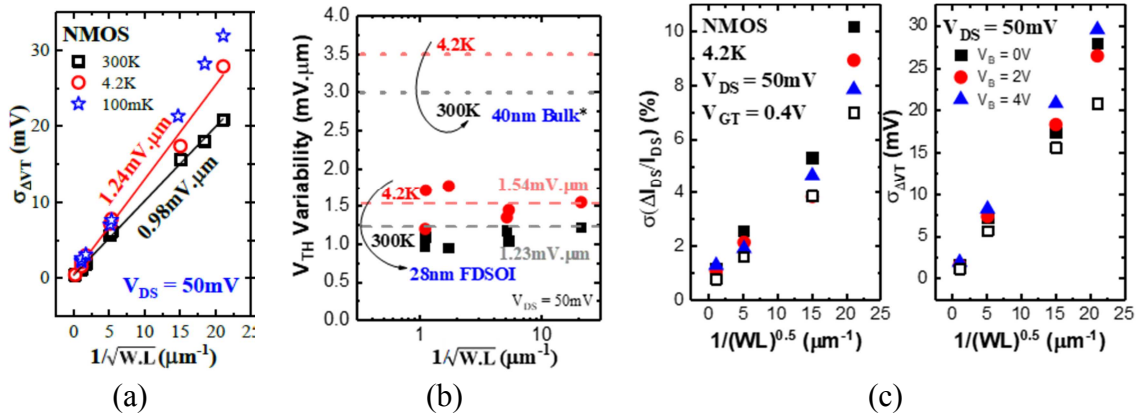


Figure 6. (a) Pelgrom plot of  $V_{\text{TH}}$  variability for NMOS ( $V_{\text{DS}}=50\text{mV}$ ) at  $T=300\text{K}$ ,  $4.2\text{K}$  and  $100\text{mK}$ . (b)  $A_{\Delta V_T}$  vs.  $1/\sqrt{W.L}$  for NMOS, at  $V_{\text{DS}}=50\text{mV}$ ,  $T=4.2\text{K}$  and  $300\text{K}$ . Dashed lines indicate the extracted linear slope values from the Pelgrom plots. Dotted lines indicate 40nm bulk CMOS technology (23). (c) *left* -  $\sigma(\Delta I_{\text{DS}}/I_{\text{DS}})$  vs.  $1/\sqrt{W.L}$  measured on NMOS ( $V_{\text{DS}}=50\text{mV}$  and  $V_{\text{GS}}-V_{\text{TH}}=0.4\text{V}$ ) varying  $V_B$ . *right*- corresponding  $\sigma(\Delta V_T)$  vs.  $1/\sqrt{W.L}$  ( $V_{\text{DS}}=50\text{mV}$ ). FBB slightly reduces  $I_{\text{DS}}$  variability, without significant impact on  $V_{\text{TH}}$  variability.

this degradation is not dramatic. For instance at 4.2K, the individual matching parameter ( $iA_{VT}$ ) of NMOS GO1 transistors increases from  $0.98\text{mV}\cdot\mu\text{m}$  at RT to  $1.24\text{mV}\cdot\mu\text{m}$  at 4.2K, which remains low (Fig.6). Such degradation has also been observed on other technologies with roughly the same extent (16),(17). This degradation at low temperature has been attributed to the impact of disorder-induced band tail states, with energies located close to the bottom of the conduction band and the top of the valence band (18),(19). Indeed, around  $V_{TH}$ , the Fermi level of the channel probes these band tail states at low temperature leading to additional fluctuations of  $V_{TH}$ , in correlation with the sub-threshold slope saturation (20),(21) or the excess  $1/f$  noise (22). The effect of  $V_B$  on current and  $V_{TH}$  variability is illustrated in Fig.6c for a NMOS GO1 transistor at 4.2K. We see that the  $V_{TH}$  mismatch does not depend on  $V_B$  at 4.2K, as at RT (13). On the other hand, a FBB can help reduce the drain current variability, especially at high  $V_{GT}$ .

Bias temperature instabilities (BTI) is one of the mechanism which can limit the reliability of transistors. BTI degradation is generally described by a thermally activated model, so that the  $V_{TH}$  shift due BTI is expected to decrease with  $T$ , and disappear at sufficiently low temperature. Ultra-fast BTI measurements have been performed on NMOS and PMOS devices at cryogenic temperature down to 4.2K (24).

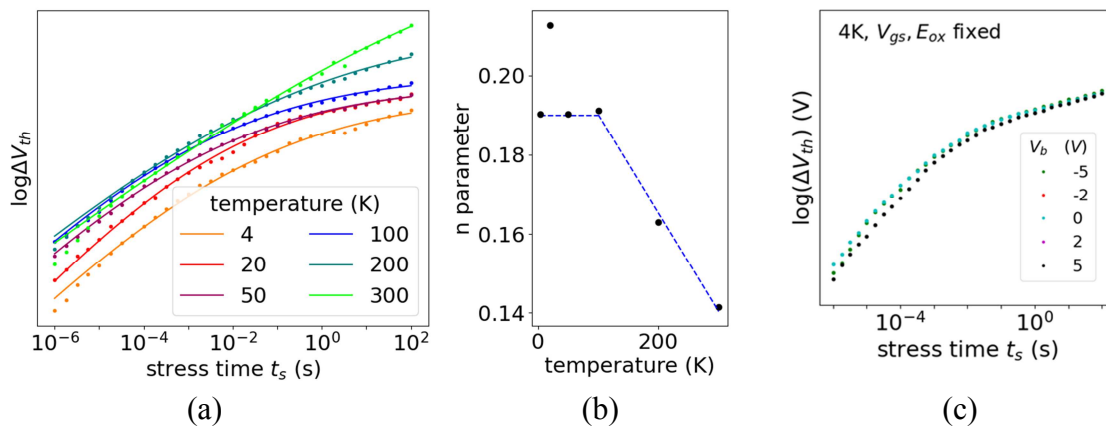


Figure 7. (a) Measured shift in the threshold voltage during PBTI stress ( $\Delta V_{TH}$ ) as a function of stress time (symbols), and corresponding curves fitted with a classical stress model (see Eq.2). (b) Evolution of the parameter  $n$  with  $T$  of the classical model. (c) Shift in the threshold voltage during PBTI stress measured at 4K at different  $V_B$  at constant oxide field  $E_{OX}$ .

We identified two regimes of temperature dependence for the time acceleration parameter  $n$  describing the evolution of the  $V_{TH}$  shift, due to a PBTI stress, with stress time  $t_s$  and stress voltage  $V_{GS, stress}$  following the classical model:

$$\Delta V_{TH}(t_s, V_{GS, stress}) \propto \frac{1}{1 + A t_s^{-n} V_{GS, stress}^\gamma} \quad [2]$$

From 300K down to 100K,  $n$  varies linearly with  $T$ ; below 100K,  $n$  saturates, indicating a change in the dominant physical mechanism responsible for the PBTI degradations. At room temperature, the degradation is mostly due to a thermally activated phenomenon (a non-radiative multi-phonon process). On the contrary, at low temperature the dominant source of degradation does not depend on temperature anymore, as is the case for elastic tunneling of carriers from the channel to traps in the gate oxide. Similar results have been observed for bulk CMOS NMOS transistors(16), confirming the remaining of a temperature-independent trapping mechanisms that dominates below

100K. To go further, we evaluated the effect of a back bias on PBTI degradation (Fig.7c). We did not observe any significant dependence with  $V_B$  at 4.2K, for  $V_B$  ranging from -5V to +5V. Therefore, back bias can be an efficient knob to mitigate BTI stress by reducing the gate voltage used to operate transistors without additional degradation induced by  $V_B$ .

### Overall performances at low temperature

**TABLE I.** Benchmark of NMOS performances at 300K and 4.2K: 28nm FDSOI (this work) vs. 40nm (23) & 28nm Bulk CMOS (16).

		This work 28nm FDSOI L = 28nm		40nm Bulk L = 40nm		28nm Bulk L = 28nm	
		300K	4.2K	300K	4.2K	300K	4.2K
$V_{TH}$ (V)	$V_B=0V$	0.29	0.49			0.31	<b>0.41</b>
	<b><math>V_B=2V</math></b>		<b>0.29</b>				
$I_{ON}/W$ ( $\mu A/\mu m$ )	$V_B=0V$	689	790	442	<b>500</b>	694	<b>893</b>
	<b><math>V_B=2V</math></b>		<b>1088</b>				
$I_{OFF}/W$ (pA/ $\mu m$ )	$V_B=0V$	900	<0.01*				
	<b><math>V_B=2V</math></b>		<b>&lt;0.01*</b>				
SS (mV/dec) @ $V_{DD}$		74	<b>4.8</b>	88	<b>28</b>	89	<b>20</b>
Weak inversion:							
$g_m/I_{DS}$ ( $V^{-1}$ )		31.2	<b>300</b>	27	<b>92</b>		
$A_V$ (V/V)		27	<b>36</b>	20.8	<b>23</b>		
$A_{VT}$ (mV, $\mu m$ )		0.98	<b>1.24</b>	3.0	<b>3.5</b>	1.85	<b>2.02</b>
$A_{\Delta\beta/\beta}$ (%, $\mu m$ )		0.51	<b>0.74</b>	0.46	<b>0.91</b>		

Table I summarizes the evolution of the overall performances of FDSOI transistors when temperature is decreased from RT to 4.2K. The back bias ability clearly brings an advantage over bulk technologies to improve and optimize LT operation of transistors, and more generally of circuits, like demonstrated for instance on ring oscillators (25) or a transimpedance amplifier (3).

### Transistor modeling

Modeling issues are addressed in this part. Besides serious numerical difficulties due to singularities appearing at low temperature when solving model equations (5), the change of important physical parameters (like carrier mobility, thermal conductivity,...) needs to be correctly taken into account in future compact or analytical models. In addition, new physical effects evidenced at low temperature also need to be understood, analytically modeled and included as well.

### Effect of back bias on the electrostatics and transport properties of the FDSOI transistors

We have evidenced that  $V_B$  modifies the transfer characteristic  $I_{DS}$  vs.  $V_{GS}$  of NMOS GO1 and GO2, especially for long channel transistors, as illustrated in Figs.8&9. At low temperature (typically for  $T<100K$ ), when  $V_B$  is biased in FBB, the drain current exhibits humps in  $I_{DS}$ , at given values of  $V_{GS}$ . These values correspond exactly to the voltage bias for which a new energy subband becomes populated by electrons (Fig.8). As a consequence, intersubband scattering (IS) can occur, and the electron mobility suddenly drops (26). This is a specific feature arising at low temperature, and associated with thin film devices (27). This effect, which becomes observable at  $T<100K$ , can be mitigated on



shorter L (Fig9b) – due to ballistic transport – and at high  $V_{DS}$  (28). Intersubband scattering could not be evidenced on our PMOS, which could be explained by the lower effective mass of holes in Si. On the transconductance curves  $g_m$  vs.  $V_{GS}$ , these humps leads to oscillations, with negative values of  $g_m$  (Fig.9a).

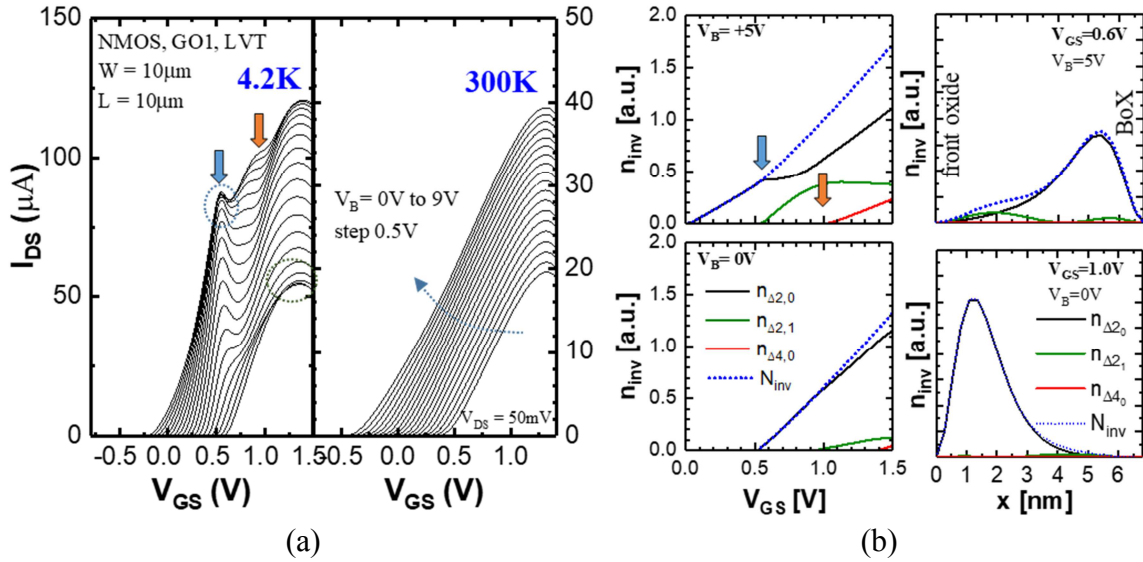


Figure 8. (a)  $I_{DS}$  vs.  $V_{GS}$  measured on a long NMOS GO1 transistor at  $T=4.2K$  and  $T=300K$ . and for different FBB values from 0V to 9V. At 4.2K and in FBB,  $I_{DS}$  exhibits two humps around  $V_{GS}=0.54V$  and  $V_{GS}=0.9V$  indicated by the arrows. (b) Inversion carrier density calculated using 2D-Poisson Schrödinger solver as a function of  $V_{GS}$ , for  $V_B=+5V$  (top left) and  $V_B=0V$  (bottom left), for the first three lowest energy subbands, and inversion carrier density distribution as a function of position  $x$  in the channel for two given values of  $V_{GS}$  and  $V_B$  (right). The arrows indicate the onset of the second and third energy subband.

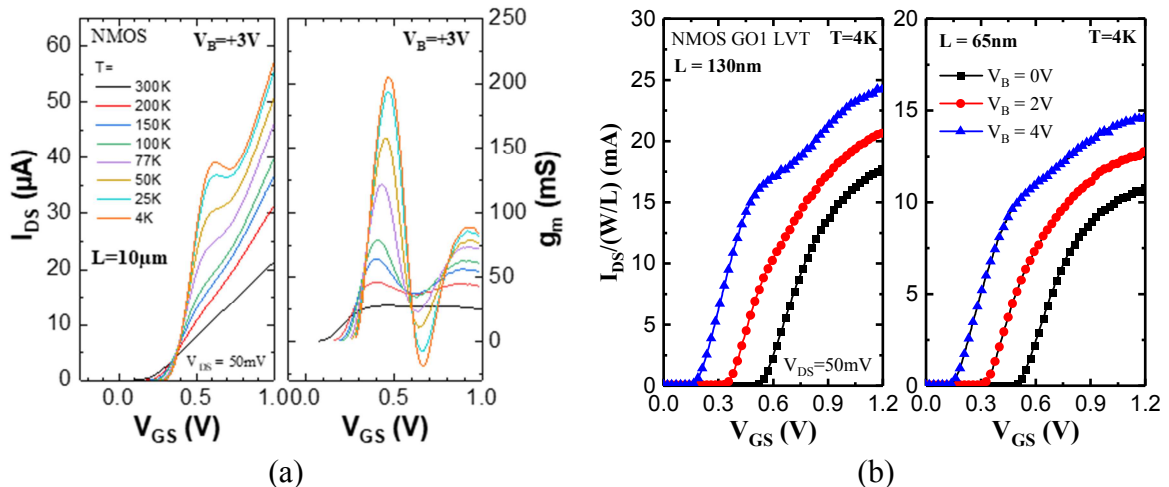


Figure 9. (a)  $I_{DS}$  measured as function of  $V_{GS}$  (left) and corresponding transconductance  $g_m$  vs.  $V_{GS}$  (right) on a long NMOS GO1 transistor ( $L=10\mu m$ ), for  $V_B=3V$ , and for different temperatures from 300K down to 4K. (b)  $I_{DS}$  vs.  $V_{GS}$  measured at  $T=4K$  on NMOS transistors with  $L=130nm$  (left) and  $L=65nm$  (right), for different  $V_B$ , showing attenuation of the IS effect.

A look at the inversion carrier density across the Si channel reveals that IS effect occurs when the front channel is opening whereas back channel was already open, and reciprocally (7) (see Fig.8b). Although the theoretical model describing intersubband scattering is known (26),(29), phenomenological equations can be used to have a more analytical model (30). In this simplified approach, front and back channel mobility can be evaluated separately at each interface with:

$$\mu_{\text{eff,tot}} = \frac{\mu_{\text{eff}1}N_{\text{inv}1} + \mu_{\text{eff}2}N_{\text{inv}2}}{N_{\text{inv}1} + N_{\text{inv}2}} \quad [3]$$

in which 1 and 2 indexes stand for front channel and back channel. Intersubband scattering can be taken into account when  $E_F > E_i$ , where  $E_i$  corresponds to the second or third subband energy level, through an additional explicit dependence of the mobility at one interface with the inversion charge density at the other interface of the form:

$$\mu_{\text{eff}2,\text{IS}} = \mu_{\text{eff}2} \left[ a + b \cdot \exp\left(-\frac{N_{\text{inv}1}}{c}\right) \right] \quad [4]$$

in which  $a$ ,  $b$  and  $c$  are fitting parameters,.

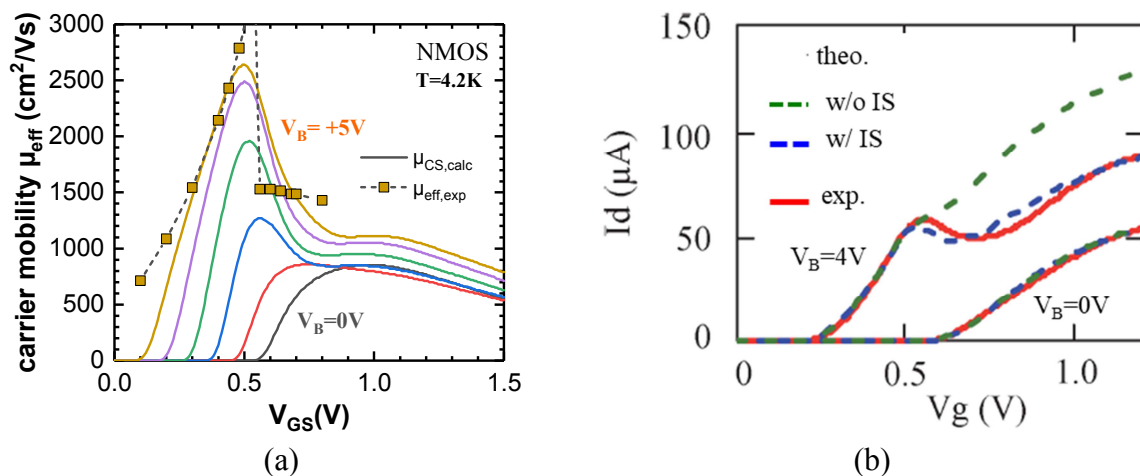


Figure 10. (a) Electron mobility extracted as a function of  $V_{\text{GS}}$  for different  $V_B$  (line), and calculated mobility with intersubband scattering at  $V_B=5\text{V}$  (symbols). (b) Drain current vs. front gate voltage  $V_g$ : Experimental (red solid line) and modeled with IS (dashed blue line) and modeled without IS (green dashed line) for  $V_B = 4\text{V}$  and  $0\text{V}$  at  $T = 4.2\text{K}$ .

Finally, Lambert-W function enables to accurately model the inversion charge and drain current from weak to strong inversion regime. We have shown that it remains valid down to ultra-low temperature, and can thus be applied for parameter extraction at low  $T$  (31).

#### Thermal effects and differential thermal resistance

Thermal effects play a fundamental role in cryogenic electronics, for which circuits are targeted to operate at various temperature stages, with limited cooling power. The study of self-heating effects at cryogenic temperature in this regard provides valuable information on how to manage thermal effects. It is also important for reliability, as it increases hot carrier degradation (32). To describe thermal effects, we extracted the differential thermal resistance defined as  $R_{\text{th}}^* = d\Delta T/dP$  (33), where  $\Delta T$  is the temperature increase in the channel of the transistor due to self-heating effect, and  $P = I_{\text{DS}} \times V_{\text{DS}}$  is the

input power. Measurements have been performed using the gate thermometry method on transistors with two-contacts gate. Our results show that  $R_{th}^*$  is strongly temperature dependent as illustrated in Fig.11a, mainly due to the temperature dependence of the Si and SiO<sub>2</sub> thermal conductivity. However, we have evidenced a strong increase of  $R_{th}^*$  below  $T \approx 75K$  by several order of magnitude on all our devices. This huge thermal resistance at very low temperature leads to a strong non-linearity of  $\Delta T$  with  $P$ , contrary to what is usually observed at room temperature (Fig.11b). The temperature of the channel measured by the gate resistance can be extracted as a function of gate voltage  $V_{GS}$ , revealing high temperature increase with respect to the ambient temperature  $T_{amb}=4.2K$ , up to 100K (7). The channel temperature in cryogenic environment can thus highly differ from the ambient temperature. This temperature increase needs to be taken into account when analyzing electrical parameters at low temperature, in particular when considering the saturation velocity or to extract the correct temperature dependence of the drain current.

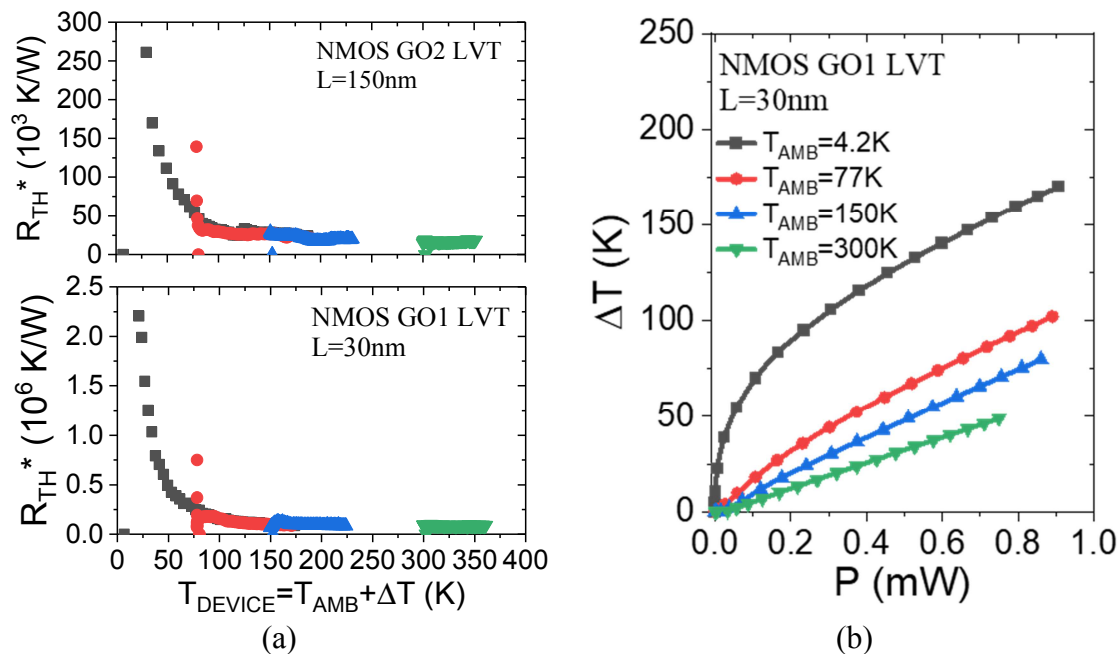


Figure 11. (a) Differential thermal resistance  $R_{TH}^*$  vs.  $T_{dev}=T_{amb}+\Delta T$  extracted by the gate resistance method on NMOS GO1 (bottom,  $L=30nm$ ) and NMOS GO2 (top,  $L=150nm$ ) showing a strongly T-dependent behavior, with a high increase below  $T=75K$ . (b)  $\Delta T$  increase in the channel extracted as a function of input power for different ambient temperatures from 300K down to 4K.

## Conclusions

We gave an overview of the extensive electrical characterization performed on 28nm FDSOI transistors down to ultra-low temperature. New physical effects arising at low temperature have been investigated and discussed, highlighting specific issues to be addressed in a future DC and RF cryogenic compact model. However, ways of optimization already exists, using the unique opportunity offered by the back bias in FDSOI technology.

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