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Experimental Study of Self-Heating Effect in InGaAs HEMTs for Quantum Technologies Down to 10K

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Abstract—This work studies self-heating effects in InGaAs cryogenic HEMT devices, which aim at the enhancement of control/readout electronics performance in quantum computers. Starting from the well-known method of gate resistance thermometry, documented in literature for its reliable results, we characterized these devices down to deep cryogenic temperatures, namely 10 K, typical of signal-processing electronics for qubits, such as low-noise amplifiers (LNA). We furthermore compared the results with those belonging to far more industrialized silicon technologies (Si FDSOI and bulk), showing exceptional performance of the InGaAs HEMTs thanks to their quantum well structure, which combined with their high electron-mobility, makes them a great study case for the technologies of the future.

Keywords – Self-Heating, HEMT, InGaAs, III-V, cryogenics, LNA, characterization

I. INTRODUCTION

Recently, interest in Quantum Computing (QC) has significantly increased. On one side, there are many efforts in developing new and more refined technologies for the actual qubits. On the other, there is also rising interest in integrating cryogenic electronics to enhance the scalability and performance of the QC. When considering the nature of QC and its architecture [1], we have to remember that some qubit technologies operate well below 1K and have a very low output signal power which needs to be amplified before going to higher temperatures and being digitized.

III-V-based high electron-mobility transistors (HEMTs) are proving great candidates for cryogenic LNA [2]; though in order to enhance their performance for future scaled QCs, their characteristics have to be thoroughly investigated down to deep cryogenic temperatures. Particularly, self-heating represents an issue that not only interferes with low-temperature-induced boost in performances but also one that gives rise to the thermal noise in the amplifier, distorting the signal from the qubit before it can be processed.

Several studies have already been carried out on self-heating, more thoroughly for Silicon (Si) devices and with an increasing interest for III-V. Particularly, Choi et al. have characterized InGaAs-based HEMTs down to 20 K [3], while Ardizzi et al. have studied GaAs HEMTs down to liquid helium temperatures analyzing the noise temperature [4]. This work will instead study InGaAs-based HEMTs down to 10 K, showing their capacity to dissipate heat and stay in line with their ambient temperature, benchmarking them moreover with well-documented Si CMOS.

II. DEVICES AND METHODS

The devices under study were fabricated by IBM Research - Zurich and consist of an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, stacked in-between two layers of InAlAs, as shown in Fig. 1. The InAlAs serves at the bottom as a buffer connecting to a semi-insulating InP substrate, and at the top as a spacer separating the channel from the delta-doping plane, and a third layer of InAlAs, to reduce possible gate leakages (Fig.1). For the present study, we tested single channel devices with channel width of 10 μm and

channel length spanning from 50 nm up to 200 nm. In all cases, the distance between source and drain regions was 1.4 μm .

As shown by Paliwoda et al., many methods have been developed to assess self-heating [5]. One of the most reliable methods is gate thermometry, which relies on 4-terminal gate resistance measurements using a custom test structure (Fig. 2). As explained in [6] and [7], the increasing temperature in the channel causes an instantaneous heating of the gate metal which is measured through the change of the gate resistance. Thus, we performed gate resistance thermometry measurements by recording the current flowing between two metallic pads connected to the gate and biased with a small differential voltage ΔV_g of 30 mV. As the drain voltage, V_d , increases and we move towards saturation region, the current ΔI_g flowing between the gate pads decreases due to an increase in resistance, caused by the self-heating of the device (Fig. 3). As we extract the gate's metal pad resistance R_g (Eq. 1) in between the pads at the beginning ($V_d = 0$ V) and the end of each measurement (Fig. 4), we can compute the temperature variation ΔT (Eq. 2), after linear regression of $R_g(T)$.

III. RESULTS AND DISCUSSION

By following the aforementioned steps, we account for the self-heating ΔT versus the dissipated power P (Eq. 3) in the channel (Fig. 5), where the linear increase of ΔT with P can provide the thermal resistance [8] R_{th} (Eq.4) by linear regression. Moreover, this allows to extract ΔT at the constant P of 1 mW, which is plotted vs temperature in Fig. 6, reporting also the values extracted at constant V_d . It can be noticed that longer channel present significant difference in ΔT according to the employed extraction, while the shorter device seems to display negligible ΔT in both cases: the channel of 50 nm is in fact sensibly shorter than the expected mean free path for these devices, which is in the order of 150-200 nm. This means that the short-channel devices are operating in the quasi-ballistic regime, and self-heating occurs mainly at the drain, rather than in the channel. Surprisingly, increased R_{th} from phonon radiation at low temperature, which is observed for Si CMOS, is not seen here. Finally, Fig. 7 demonstrates that the HEMTs under study, being bulk-like devices, have a very good heat dissipation (low R_{th}), close to state-of-the-art bulk Si CMOS [9] and much better than FDSOI MOSFETs [8].

IV. CONCLUSIONS

We have characterized self-heating effects in InGaAs cryogenic HEMTs through gate thermometry and shown that R_{th} remains fairly constant down to 10 K. The combination of a bulk structure and high mobility enables efficient heat exhaust, resulting in low levels of self-heating. The results build up the understanding of the cryogenic operation of state-of-the-art HEMTs for qubit readout amplification.

ACKNOWLEDGMENT

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EQUATIONS

$$R_g = \Delta V_g / \Delta I_g \quad (1)$$

$$\Delta T = \frac{R_{g,final} - R_{g,initial}}{dR_g/dT} \quad (2),$$

$$P = I_d \cdot V_d \quad (3)$$

$$R_{th} = \Delta T / P \quad (4)$$

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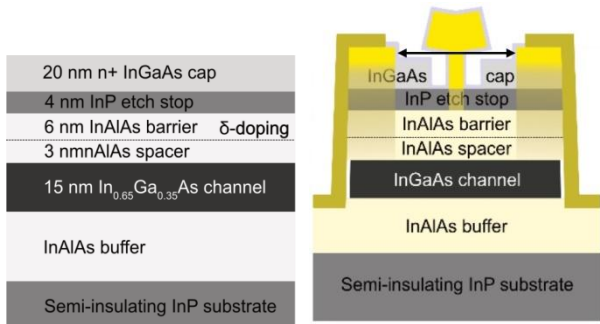


Figure 1. Schematics of the layer-stack of the HEMT devices under study

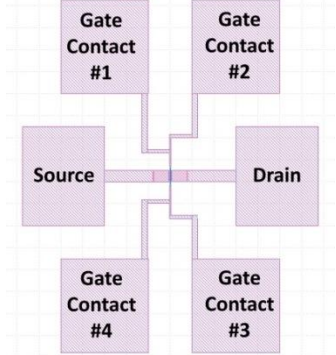


Figure 2. Schematics of the contact pads, with multiple gate-pads dedicated for gate thermometry

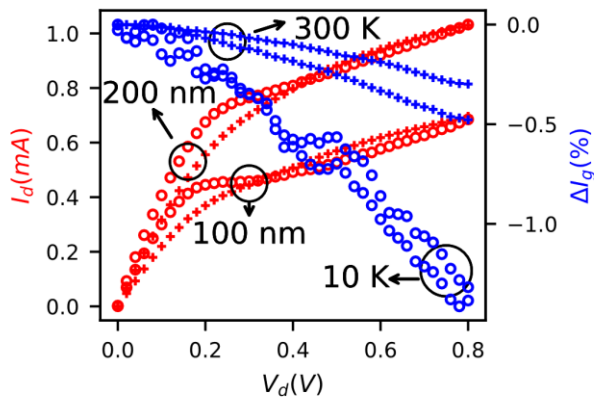


Figure 3. Raw measurement of gate resistance thermometry for $W = 10 \mu\text{m}$ and $L_g = 100$ and 200 nm at $T = 10$ and 300 K

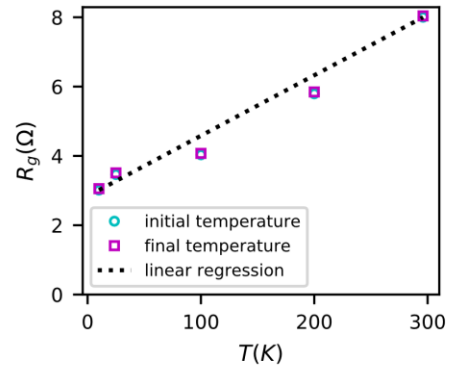


Figure 4. Resistance of the gate metal vs temperature at initial and final stages of measurement for $W = 10 \mu\text{m}$ and $L_g = 200 \text{ nm}$

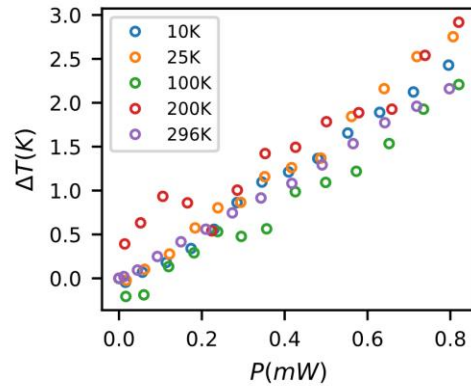


Figure 5. Self Heating for $W = 10 \mu\text{m}$ and $L_g = 200 \text{ nm}$ versus dissipated power in the channel

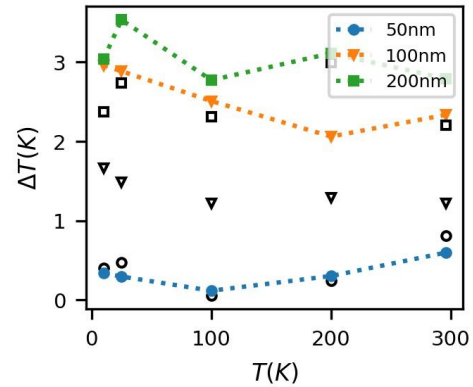


Figure 6. Extracted Self Heating for $W = 10 \mu\text{m}$ and different channel lengths versus temperature at constant- P (coloured) and constant V_d (black)

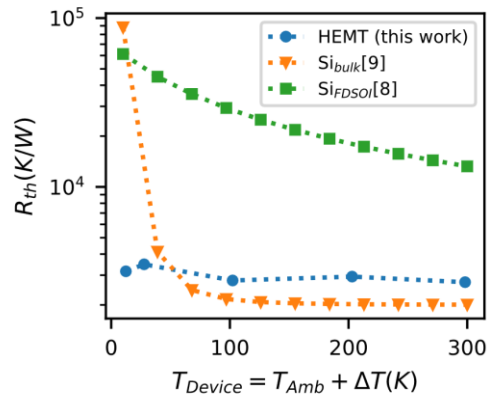


Figure 7. Thermal resistance versus temperature for different technologies.