

# SiC plasma etching technology processes for power and optoelectronic devices

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# SiC – one of the most technologically advanced wide bandgap semiconductor

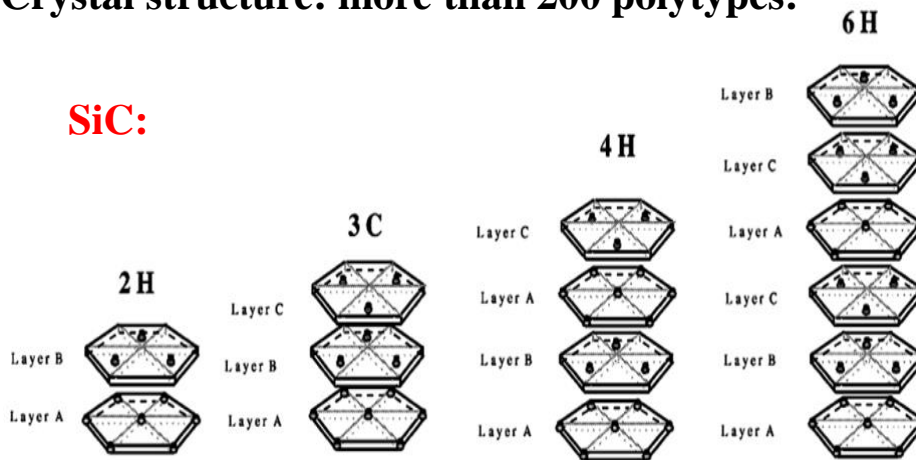
	$E_g$ (eV)	$\epsilon_r$	$\mu_n$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	$\mu_p$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	$E_c$ ( $\text{MV} \cdot \text{cm}^{-1}$ )	$v_{\text{sat}}$ ( $10^7 \text{cm} \cdot \text{s}^{-1}$ )	$\lambda$ ( $\text{W} \cdot \text{cm}^{-1} \cdot \text{K}^{-1}$ )
Si	1,1	11,8	1450	500	0,2-0,8	1	1,5
2H-GaN	3,39	9	900	350	3,3	2,5	1,3
GaAs	1,42	12,9	8000	400	0,4-0,9	0,7	0,46
3C-SiC	2,2	9,6	900	45	1,2	2	4,5
6H-SiC	3	9,7	370	90	2,4	2	4,5
4H-SiC	3,26	10	600	115	2	2	4,5
Diamond	5,45	5,5	1900	3800	5,6	2,7	20

**Electronic fields:**  
**High temperature**  
**High power**  
**Compact systems**  
**Low switching losses**  
**High-frequency**

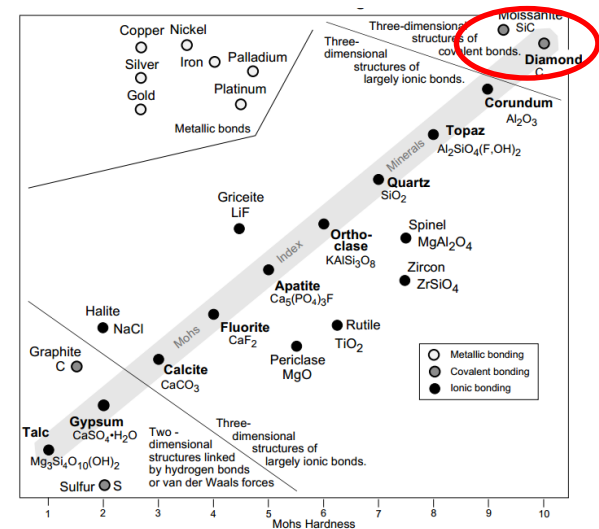
**Harsh environment**  
**Strong interatomic bonding**  
**High chemical inertness**  
**Good bio-compatibility**

Crystal structure: more than 200 polytypes:

SiC:

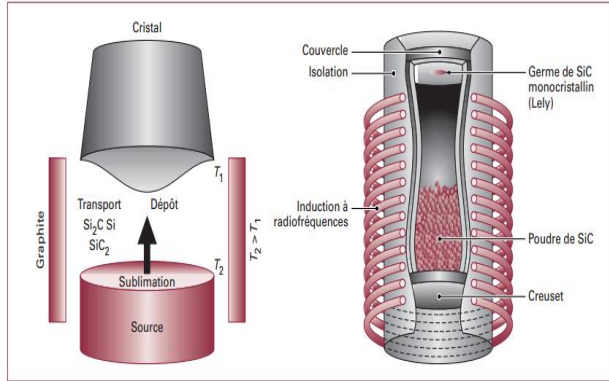


Hardness (Mohs scale)

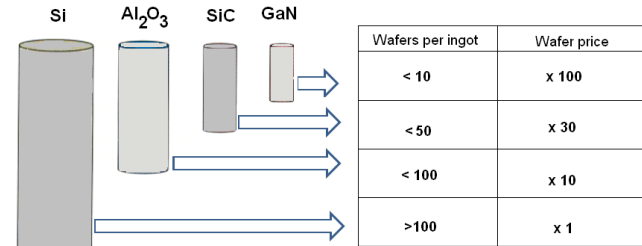


# Particular and complex processes for the growth and technology

"ingot growth" SiC~2000°C (without liquid phase)



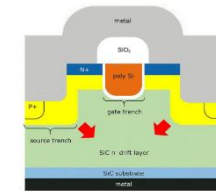
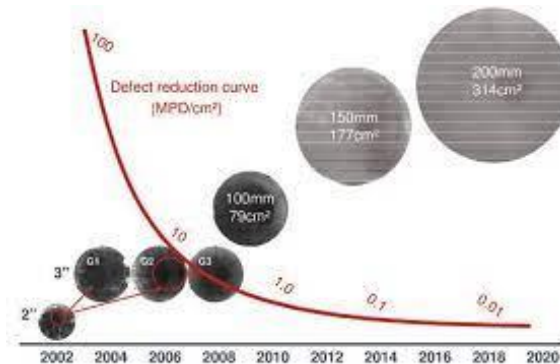
Considerable « cost »



M.A. Fraga et al, "Silicon Carbide in Microsystem Technology - Thin Film Versus Bulk Material", 2015, INTECH Ed

But remarkable industrial investments in power electronics over the last decades:

- continuous progress in reduction of defect densities,
- increase of wafer size
- and lowering of wafers costs.



MOSFET in SiC



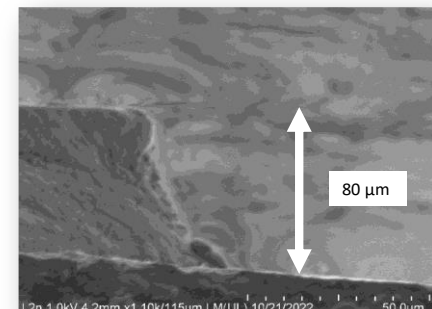
Power discrete SiC devices already commercialized (Farnell...)

## **SiC etching**

- mainly dry methods to etch SiC (ICP, RIE)**
- fluorinated plasma ( $\text{SF}_6$ ) preferred to chlorides (Ar/ $\text{Cl}_2$ )**
- wet etching does not work except by electrochemical process**

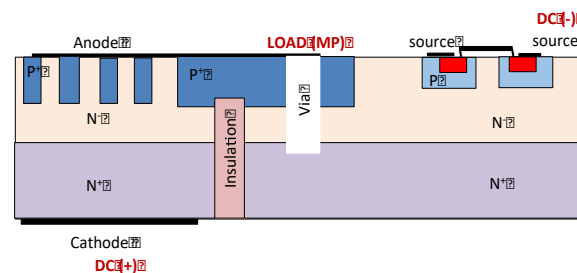
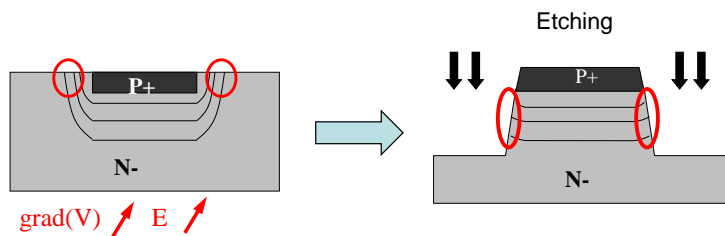
# SiC plasma etching

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# Power electronics :

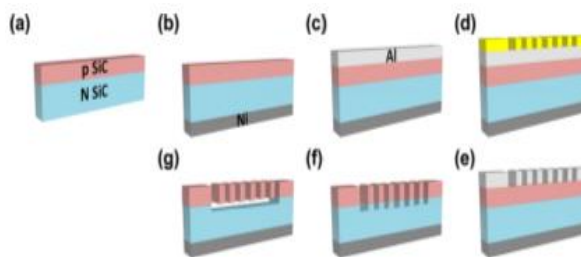
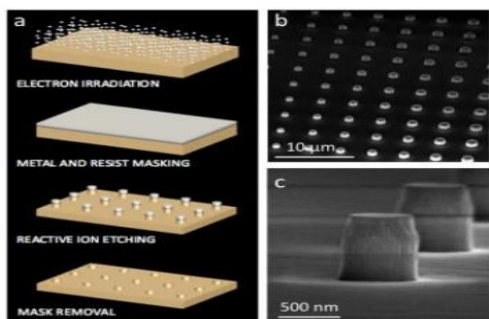
- to eliminate high electric field areas (mesa), insulation via, to transfer back side contacts in surface



~10 to 100µm minimum

# Color centers in SiC

- localize NIR luminescent defects in photonic nanocavities or µ nano-pillars



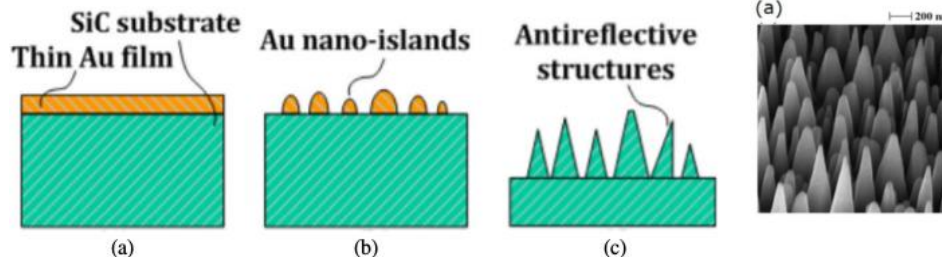
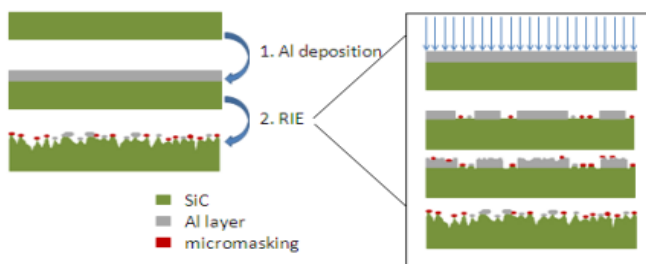
~1 à 10µm very different AR (<1µm width)

M. Radulaski IEEE Lasers and Electro-Optics (CLEO), 2017  
D. Bracher Nano Lett., 2015, 15 (9), pp 6202

# Sensors/ Detectors or LEDs

- surface nano-structuration to increase active areas/ light emission

## RIE CF<sub>4</sub>/O<sub>2</sub> "micromasking" Al/SiC



\*A. Argyraki et al., Optical Materials Express (2013) Vol. 3, No. 8 1119

\*Haiyan Ou et al., Eur. Phys. J. B (2014) 87

# SiC plasma etching – former results

Process optimized in Lyon (NanoLyon platform - INL) on several RIE

Nextral NE110



Corial 200S

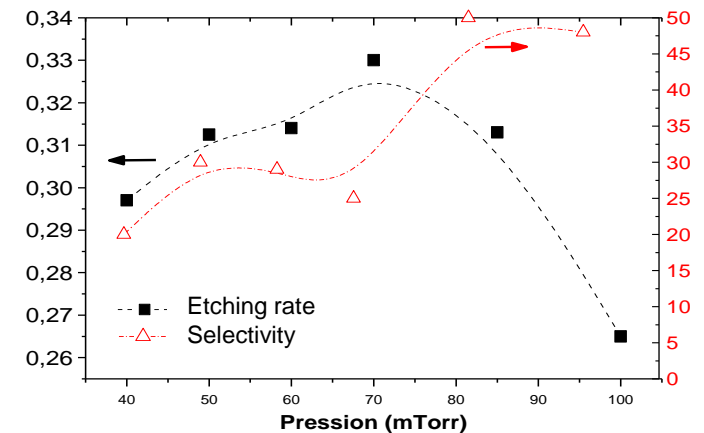
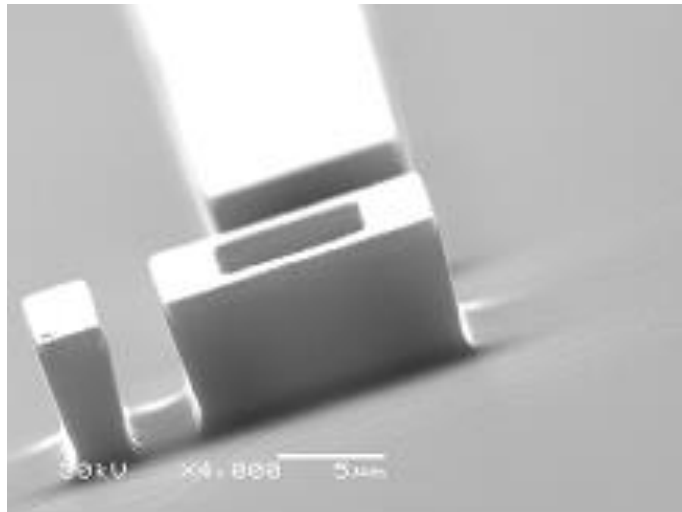


Oxford NGP80



RIE NE 110 parameters:

- $\text{SF}_6 - \text{O}_2 / 25 - 6.7$  sccm
- 250 W / 60 mTorr
- Hard mask : Si/Ni



- without trenching (on NE110)
- without micromasking
- slight **anisotropy – tilted sides** (chemical mechanisms)

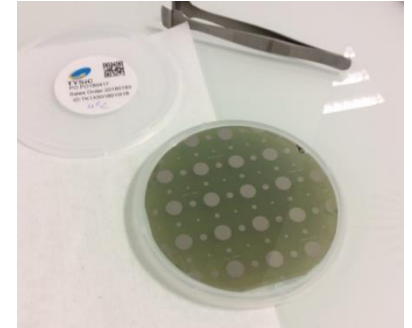
M. Lazar, H. Vang, P. Brosselard, C. Raynaud, P. Cremilleu, J-L. Leclercq et al., *Superlattices and Microstructures* 40 n°4-6 (2006) 388;

M. Lazar et al., *Materials Science Forum* Vols. 679-680 (2011) 477

# SiC plasma etching – technological transfer

Implementation of 100/150 mm SiC technological fabrication line (from 2019):  
Nano'Mat/L2n (UTT Troyes) and ESYCOM (ESIEE Paris) clean room

- access to more performants ICP/RIE equipments
- adapted to actual SiC wafer sizes (100 mm minimum)
- the possibility to increase etching thicknesses, etching rates and various shapes

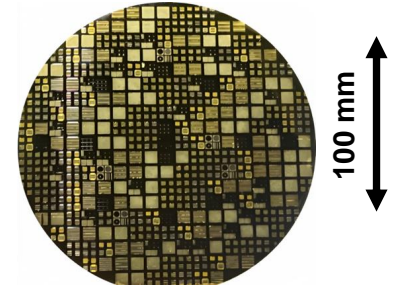




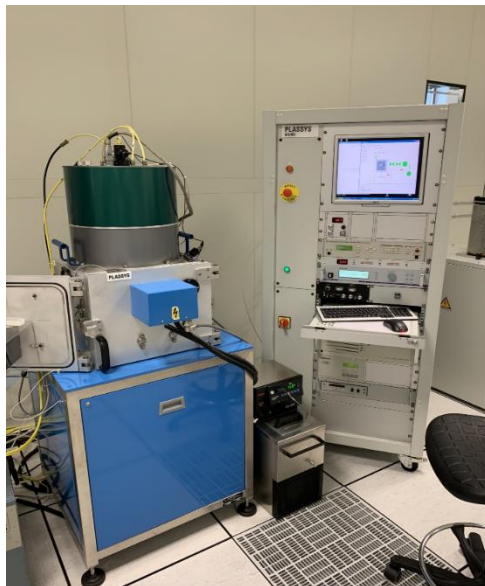
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**Plassys MUP400 :**



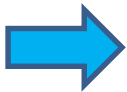
**Alcatel A601E :**



# SiC plasma etching – technological transfer

## Parameters adapted for the process on ICP/RIE equipments:

- $\text{SF}_6$  or  $\text{SF}_6/\text{O}_2$  (10 à 20%)
- Lower ICP power compared to Si process – etch rate increases up to a maximum and after decreases
- need physical mechanism (ion erosion) as chemical ones (and even more)
- High bias is necessary (several 100V)
- Pressure down to the limit of the throttle-valve control
- Not too low in order to keep good mask selectivity (Ni, Cr)
- Micromasking: improve the volatility of the etch by-products (by adding Si or C, avoiding quartz or Al support...)
- Trenching ?
- Etching rate increased x 2 - 3 ( = < 1 $\mu\text{m}/\text{min}$ )

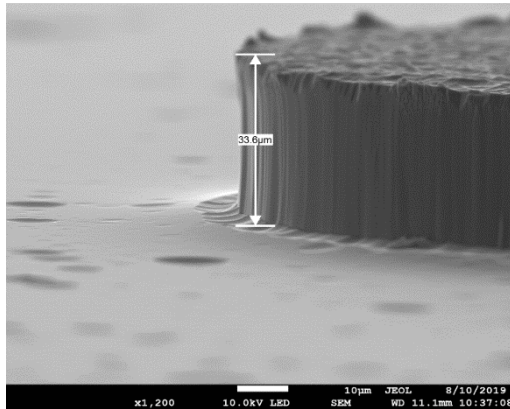


- Similar process on other WBG semiconductors  
(as GaN: Julien Ladroue phd thesis 2011 GREMI Orléans)



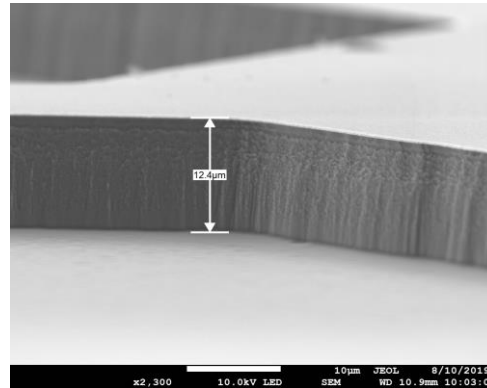
## SF<sub>6</sub> - ICP Plassys MU400 equipment from L2n – NanoMat UTT:

35 to 80 μm mesa  
and vias



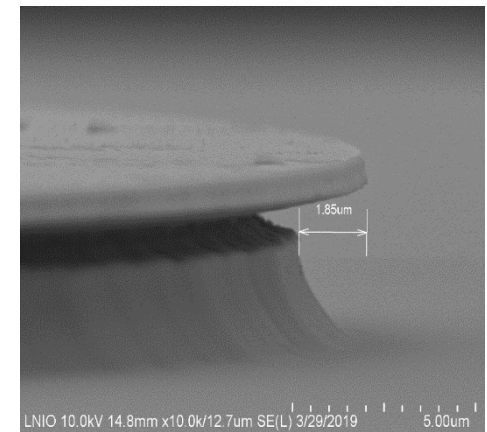
- Mask: Ni ~1 μm

10 to 15 μm to  
contact substrate



- Mask: ZnO ~1 μm  
(MUZ process)

Etching isotropy  
(of Si)

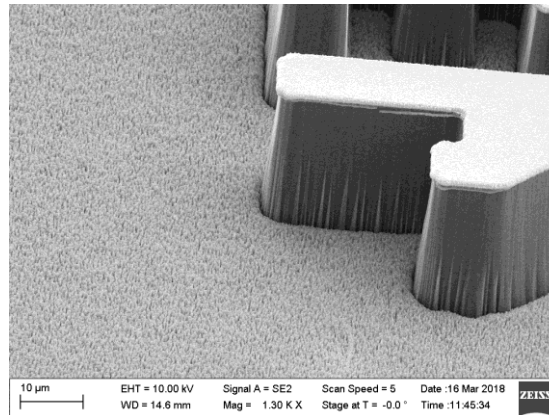
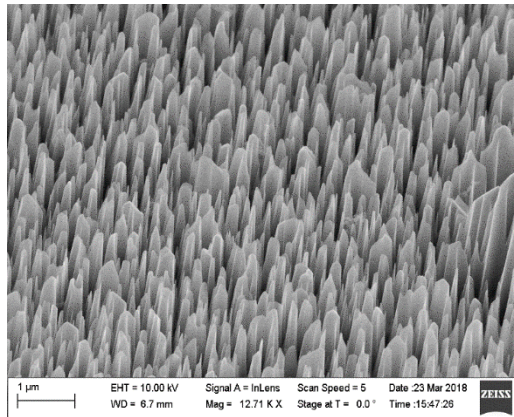


- SiC/Si substrate  
substrate

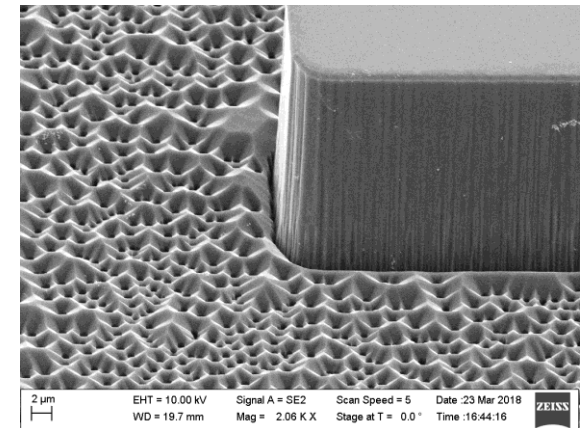
**SF<sub>6</sub>/O<sub>2</sub> - ICP Alcatel A601E equipment from ESIEE:**



**Black-SiC :**



**Orange peel texture :**



**-Trenches etched in SiC > 20μm (power devices)**

- **Nanostructuring in surface controlled by initial Ni distribution at the SiC surface (?)**
- **Control plasma energy, mask sputtering, Ni/SiC reaction**
- **Different structures on Si or C face (micromasking initial step).**

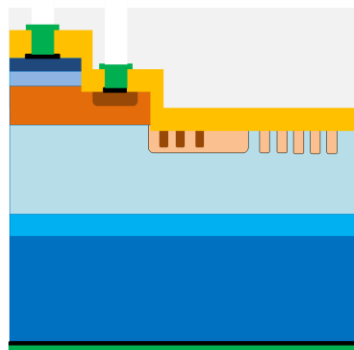


- **antireflective structures (ARS) for LEDs with color centers in complement with high temperature annealing methods**

# SiC power electronics – exemple of high voltage devices

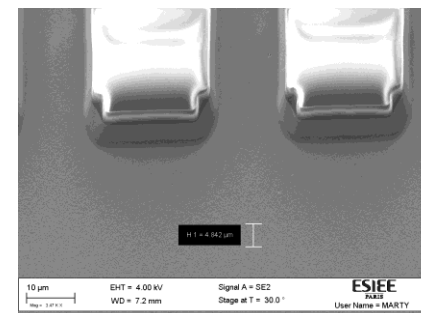
## 10 kV Photo-transistors – BJT structures

Process-flow HV-Photo SW: 11 mask levels, about one hundred steps

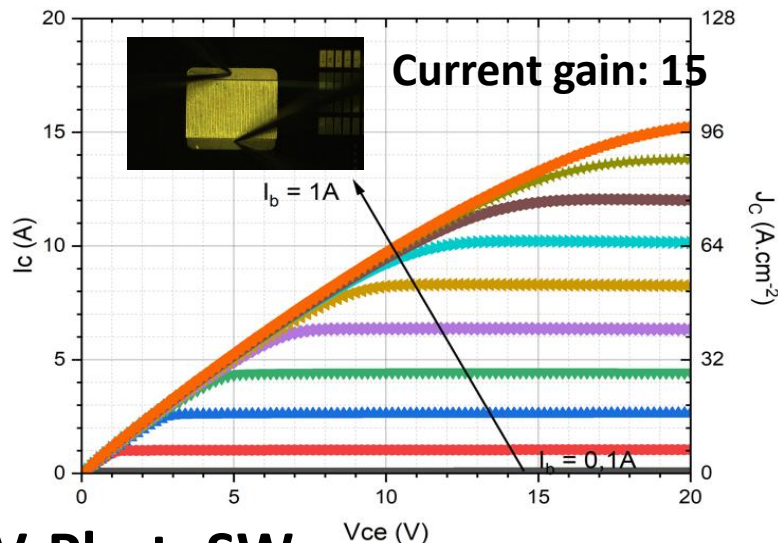


- |  |   |   |
|--|---|---|
| <span style="color: blue;">■</span> N <sup>++</sup> contact (épi)          | <span style="color: orange;">■</span> JTE (impl)                | <span style="color: black;">■</span> Métallisation fine       |
| <span style="color: lightblue;">■</span> N <sup>+</sup> sous-contact (épi) | <span style="color: lightblue;">■</span> N <sup>+</sup> (épi)   | <span style="color: green;">■</span> Surmétallisation         |
| <span style="color: orange;">■</span> P <sup>+</sup> base (épi)            | <span style="color: cyan;">■</span> N <sup>+</sup> buffer (épi) | <span style="color: yellow;">■</span> Passivation 1           |
| <span style="color: brown;">■</span> P <sup>++</sup> base contact (impl)   | <span style="color: blue;">■</span> N <sup>+</sup> substrat     | <span style="color: grey;">■</span> Passivation 2 (polyimide) |

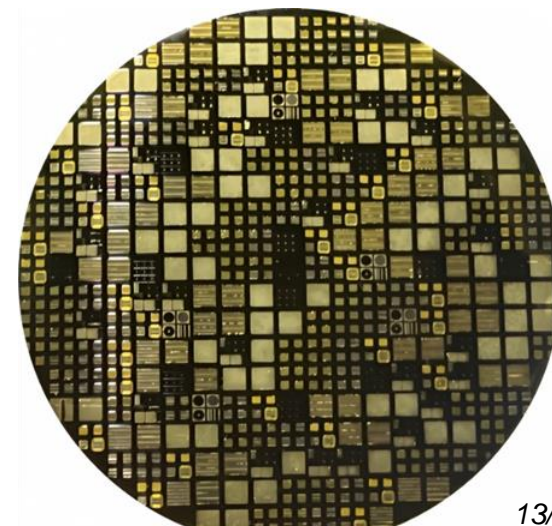
- SiC dry etching (emitter, base)
- Al ion implantation (JTE, base)
- Ohmic contacts (n and p-type)
- Mask and passivation (SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>), opened by dry etching
- Surmétallisation
- Polyimide



5 mm x 5 mm electrical BJT

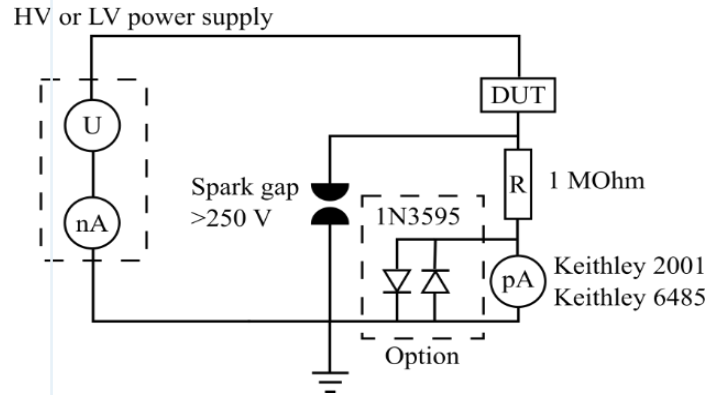


100 mm processed SiC wafer

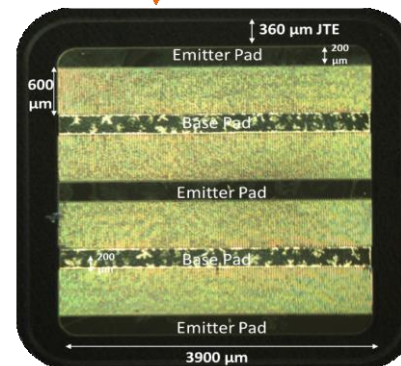
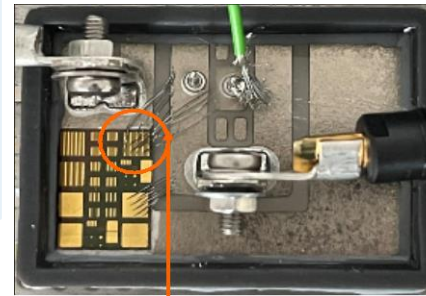
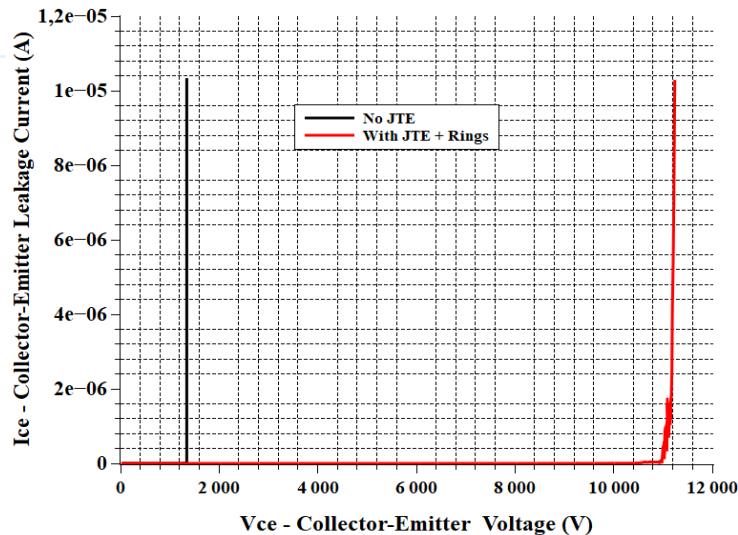


# 10 kV BJT Photo-transistors

Breakdown voltage: 11kV (the goal was 10kV)



Reverse IV characteristics - open emitter blocking



Electroluminescence at high voltage

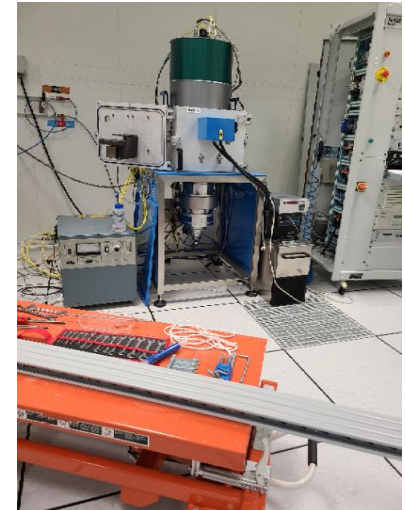
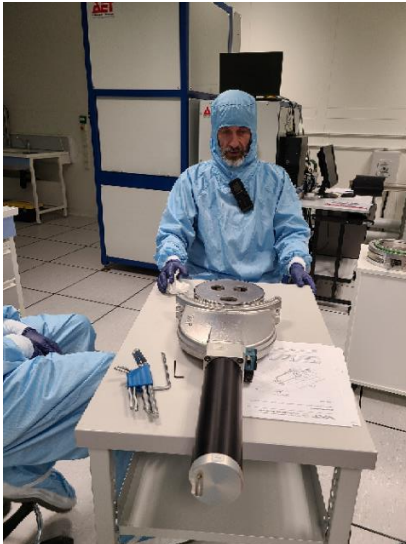


# SiC dry etching – limits of current equipments

## Plassys MUP400 :



- major breakdown (6 months) - PLASSYS intervention
- repeated 3 months later ...
- $\mu$ -crack in a cooling Al holder
- finally found and fixed it (Thanks Sergei!)



# SiC dry etching – limits of current equipments

Alcatel A601E :



- No more Ni masks . Ni forbidden due to other process contamination.
- No more deep SiC etching



- Quite old and tired set-ups or utilized with standard processes which not support contaminations

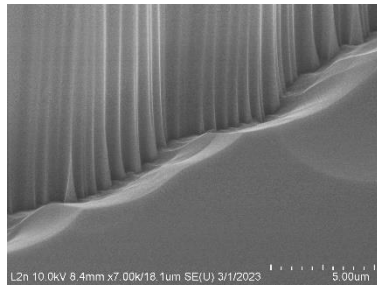
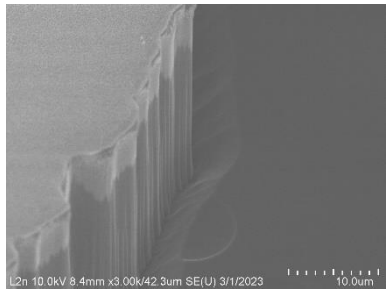


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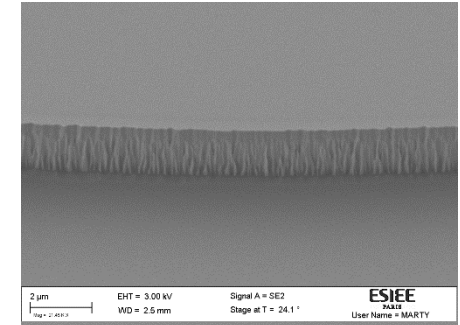
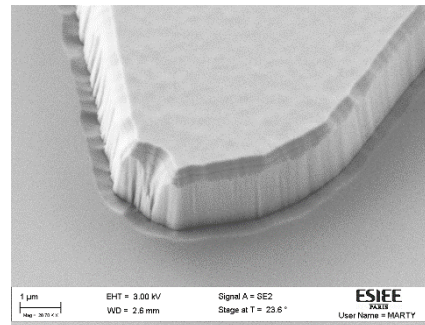
Process transferred to more recent equipments – in order to duplicate the present ones - purchases in progress

- CORIAL 200 IL – GREMI Orléans (process optimized)
- OXFORD Plasmalab – ICB Dijon (process adapted)
- SENTECH SI500 – INL NanoLyon – ECL Ecully (process adapted)
- CORIAL 210 IL (Plasma-Therm) – ESIEE Paris (process adapted)

## Corial 200 IL

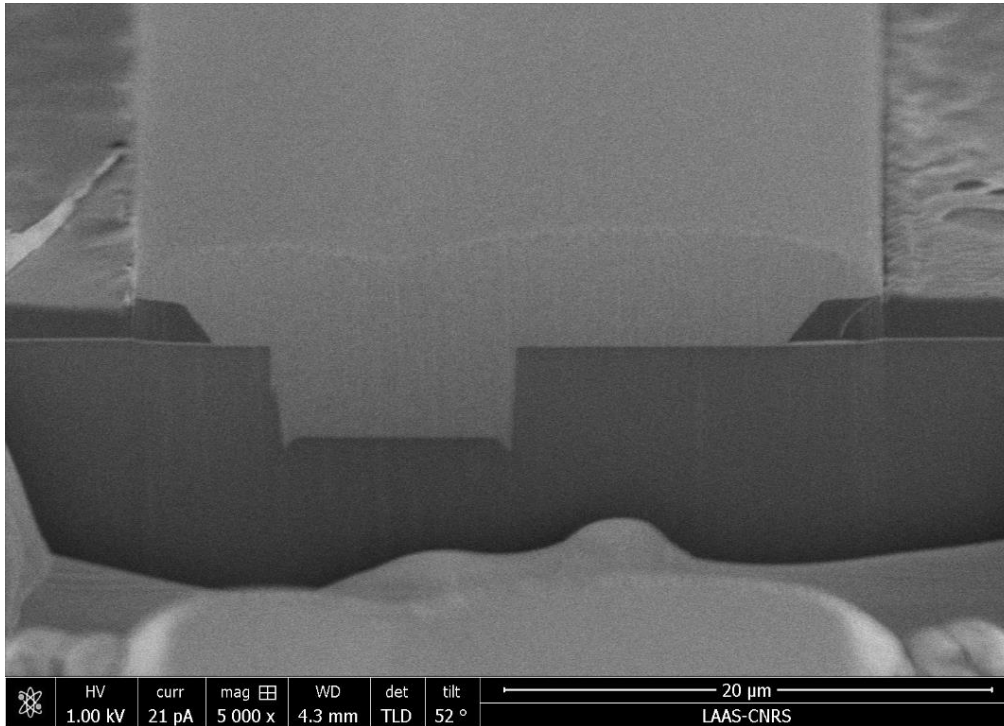


## Corial 210 IL (SiO<sub>2</sub> mask)



- Trenching is not eliminated completely
- Even by using masks with lower selectivity (SiO<sub>2</sub>) on Corial 210 IL Plasma-Therm

# SiC dry etching – trenching



- SENTECH SiC etching (Lyon)
- Ni seed layer- sputtering (ESIEE Paris)
- Ni Electroplating and FIB (LAAS Toulouse)

anr<sup>®</sup> MUS<sup>2</sup>iC



- The trenching were well eliminated only on two set-ups
  - Nextral NE110 (RIE)
  - PLASSYS MU400 (ICP/RIE)

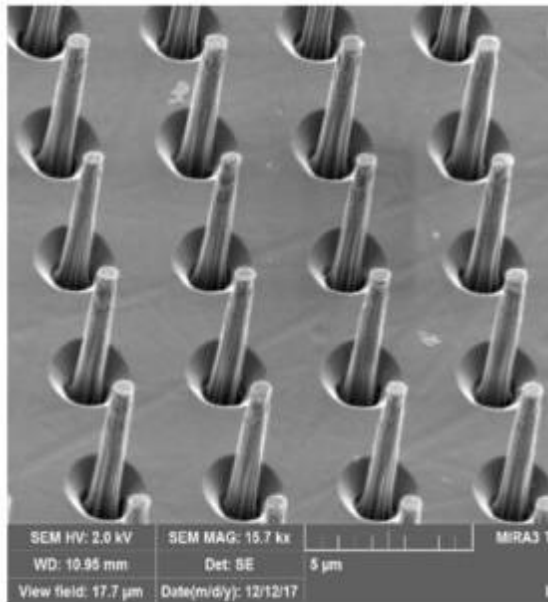
# SiC dry etching – trenching

$\mu$  Nano-pillars fabrication in SiC to enhance light collection from color centers



Corial 200 S

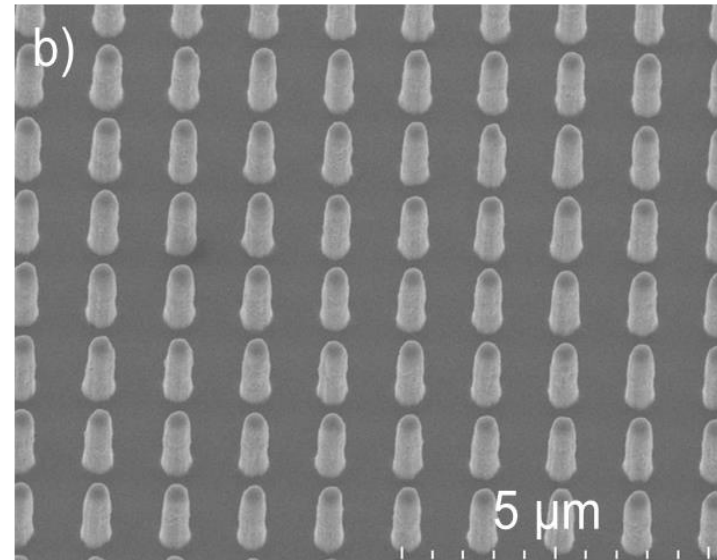
AL ATEM – INL INSA Lyon (Phd thesis 2018)



PLASSYS MU400



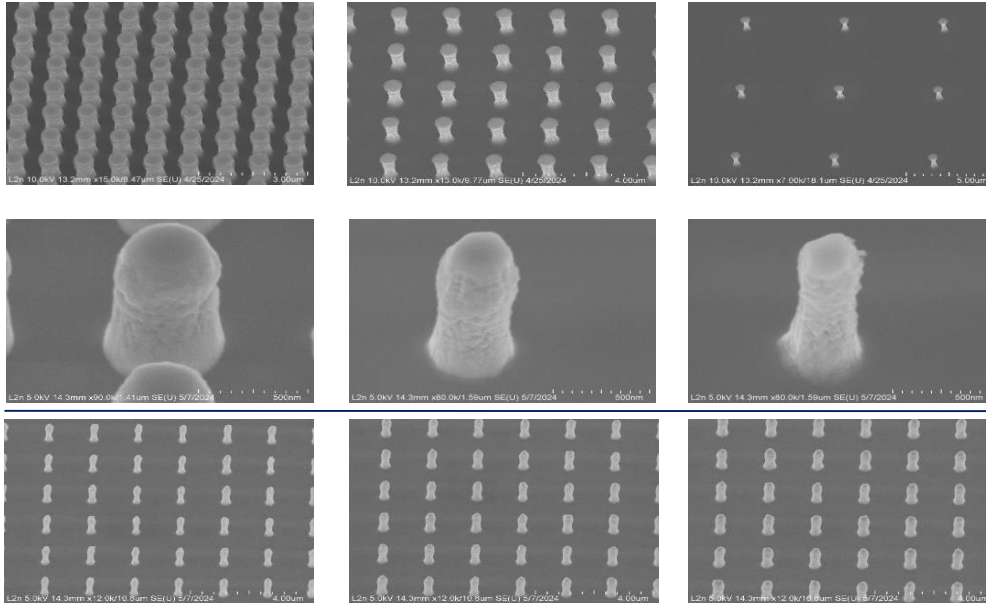
E. VUILLERMET – L2n UTT (Phd thesis in progress)



# SiC dry etching – lateral etching

$\mu$  Nano-pillars fabrication in SiC to enhance light collection from color centers

PLASSYS MU400

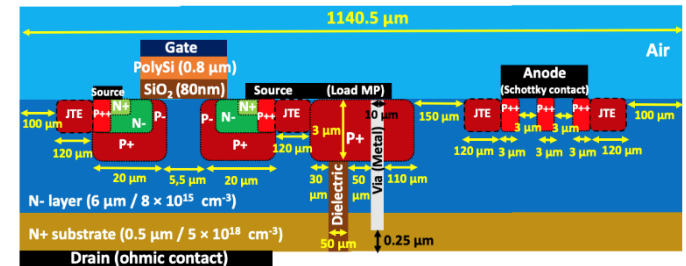


Diameters (nm)							
$D_{th}$	$D_B$	$D_T$	$S_{245}$	$S_{335}$	$S_{540}$	$S_{945}$	$S_{5000}$
700	700	550	550	530	500	470	410
650	650	500			490	410	
600	600	450			450	350	
550	550	400			390	260	

# SiC dry etching – etching rates

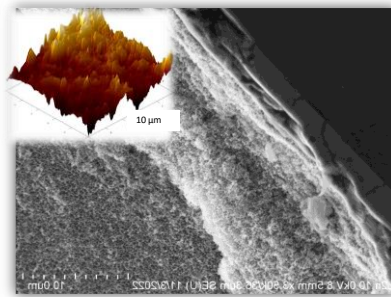
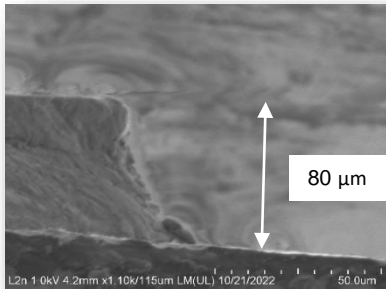
Etching rate limit:  $\sim 1\mu\text{m}/\text{min}$

- Integration of vertical power devices needs insulation through the entire substrate -  $350\mu\text{m}$
- Ni or Cr mask consumed
- Duration limited to 20-30 min

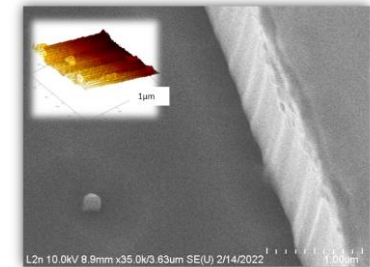
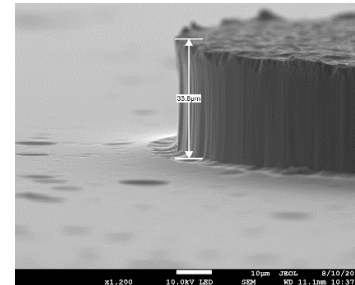


anr<sup>®</sup> MUS<sup>2</sup>iC

Wet electrochemical etching (KOH)



Plasma etching



Solution today:

- Combine alternatively plasma and wet electrochemical etching

Thank you for your attention